User's Manual

Of

Advantech RISC SOM-A2558 Series Module

System Module with *Intel XScale PXA255* **processor,** *Advantech EVA-C210 I/O enhancement Chip* **with Windows**[®] **CE.NET**

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http://www.advantech.com/risc

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ABSTRACT

This manual describes the SOM-A2558 series module functions.

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2

Revision History

Version	Date	Reason
V1.00	2004.05.19	1st Official released version. (For 9696255201, 9696255801, 9696255F01 & 9696255F12)

Chapter 1 SOM-A2558 series Architecture
## 1.1 Introduction

Advantech SOM-A2558 module uses a dual-chip design principle. SOM-A2558 series System On Module integrates both an Intel XScale PXA255 ultra low power CPU with Advantech's EVA-C210 companion chip. This offers the advantage of integrated controllers, but with multiple I/Os, such as CF, PCMCIA, USB Host, USB Client, RS-232/UART, PCI Bus Rev. 2.2, 10/100Base-T Ethernet, PS/2 ports and RS-485.

SOM-A2558 series Design highlight:

- 68 mm x 68 mm x 6.8 mm compact size module
- Power management ready support with Normal, Idle, Suspend, Off mode utilities.
- OS-ready package for Windows CE .NET/Linux Installation (Windows CE .NET 4.2 BSP ready)
- Local bus(AMI Bus), comprehensive I/O interfaces as PS/2 port, Ethernet, USB Host and PCI I/F support
- Boot option by onboard Flash or CFC makes easy maintenance and cost savings
- Provide a variety of reconfi guration options to fulfi ll specifi c requirements
- Design-in Kit package is available for complete design-in support
- Optional RISC CE-Builder assists for customer own image development

SOM-A200 architecture

SOM-A255x series are based on Advantech SOM-A200 architecture to design. SOM-A200 is Advantech RISC ultra-low power series SOM architecture. The following block diagram is the SOM-A200 architecture.

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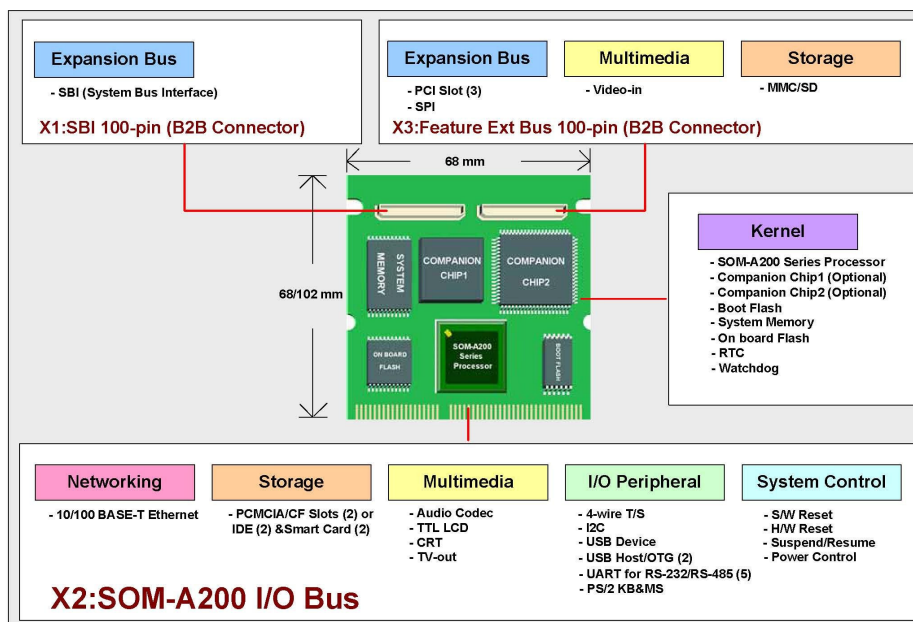
Based on SOM-A200 architecture to design, SOM-A255x (SOM-A2552, SOM-A2558 and SOM-A255F) series have two kinds of PCB form factors.

- SOM-A2552 & SOM-A2558 series: 68mm x 68mm x 6.8mm
- SOM-A255F series: 68mm x 102mm x 6.8mm

SOM-A2558 benefit

The SOM-A2558 series are very compact (68mm x 68mm x 6.8mm) and highly integrated system module. SOM-A2558 series products have a standardized form factor and standardized connectors (DDR-SODIMM Memory Connector and two 100-pin board-to-board connectors) that carry a specified set of signals. This standardization allows users to create application-specified User Solution Board **(CSB)** which can accept a variety of present and future SOM-A200 series modules.

SOM-A2558 series include popular & common peripheral functions such as serial ports, LAN, USB, PCI, etc. The CSB designer can optimize exactly how each of these functions is physically implemented. Connectors can be placed precisely where they are needed for the application, on a baseboard designed to optimally fit the system configuration and layout.

A CSB design may be used with a range of SOM-A2558 modules. This flexibility can be used to differentiate products at various price/ performance points, or to design "future proof" systems that have a built-in upgrade path. The modularity of an SOM-A2558 solution also insures against obsolescence as computer technology continues to evolve. A properly designed SOM-A2558 CSB can be used with several successive generations of SOM-A2558 modules. An SOM-A2558 CSB design thus has many of the advantages of a custom computer board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

Based embedded platform integrates both **low-level hardware and software** design and is always agreed to require heavy R&D resources, huge development effort, risk as well as long time to market lead-time. Moreover, the fast develop RISC SoC technology and short product life that has been challenging System Integrators how to make a right product development approach while foreseeing the huge advantage & benefit by adopting RISC-base solution.

SOM-A2558 series are an innovate platform architecture of WinCE.NET-**ready complete functional system** in a low profit module with SODIMM **200-pin** unified **I/O ready bus** interface that is designed to fit into application-specified User Solution Board **(CSB)** with easy, risk-less, robust, fast implementation approach. Dual expansion interface and Pre-select Embedded OS also are well integrated on module. OS Board Support Package **(BSP)** and advantech own-develop system utility & tools are also supported for an **easy design-in** business philosophy.

SOM-A2558 series Application

SOM-A2558 series is designed for Ideal for power critical & I/O intensive required base Applications

- Mobile, battery-powered device platform with multi-I/O I/F demands

5

- Compact diagnostic, monitoring, control equipment or HMI terminals
- Outdoor, fully enclosured, Intelligent remote I/O controllers
- LCD-based vehicle/telemetric platforms for navigation & communication.

SOM-A2558 series design-in package

The Design-in Kit package provides developer complete reference design-in suit for **application evaluation/ development** and own **Customer Solution Board (CSB)** development. It contains the needed information, documentation and tools for starting their hands-on work as the followings items:

- **Target SOM (SOM-A2558-440B0)**: SOM-A2558 standard version board.
  SOM-A255x series Reference Carrier Board (RCB): Sample CSB for developer reference. The board can be used in SOM-A255x series board. (SOM-A255x means SOM-A2558, SOM-A2558 and SOM-A2558)
- **64MB compact flash card :** the CF card is empty without any file inside.
- **SOM-A255x series support CD :** includes
  - sample image & boot loader
  - manuals & datasheets
  - SOM-A255x series CSB design guide
  - S/W utility(upgrade utility, testing utility)
  - SOM-A255x series WinCE 4.2 BSP & SDK
  - Application note
- **Testing Set**:
  It is designed for sample CSB or user own CSB/mass production test. It includes:
  - **H/W testing tools:** RS232 loop-back testing tool, ADAM-4520 for RS485 testing, null MODEM cable, JTAG cable, USB ActiveSync cable, Audio cable, RS232 cable and RS485 cable.
  - **S/W testing Utility:** Advantech-developed testing Utility. Testing process will be implemented by S/W testing Utility and H/W testing tools.
  - **Document:** *"User's manual of SOM-A255x series testing kit".* User can base on the documents to know how to implement testing process.
- **Software Development Tools:**
  Software tools is the complete package for user developed their target image to align with their target CSB and applications
  - **BSP:** Binary Board Support Package of target SOM Design-in Kit. User can integrate their target WinCE platform in components & Apps & drivers
  - **SDK:** For user target Apps development
  - **Reference Image:** Reference Image for the selected model of SOM.
  - **Bootloader:** Bootloader for the SOM-A255x series board.

6

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- **Upgrade Utility:** User can use Upgrade utility to upgrade boot logo, image & bootloader.

Except the Design-in package, Advantech also supply many types of LCD kits for users to reduce their developing effort. The LCD kit include the following items:

- LCD
- Inverter
- Cables: includes LCD signals cable, Inverter signals cable.
- Document: The LCD kit installation guide.

Advantech supply the following LCD kits for user to choose

- **LCD-A057-STQ1-0 (Optional item)**
  5.7" STN QVGA LCD kit. The kit includes 5.7" STN QVGA LCD (NAN-YA/ LCBFBTB61M23), 4-wires resistive T/S, inverter, cables and installation guide. SOM-A2552 & SOM-A255F series don't support 320*240 STN panel in this moment, if user have this kind of requirement, please contact with ae.risc@advanch.com.tw or advantech regional sales for further support.
- **LCD-A064-TTV1-0 (Optional item)**
  6.4" TFT VGA LCD kit. The kit includes 6.4" TFT VGA LCD kit(PRIMEVIEW PD064VT2), 4-wires resistive T/S, inverter, cables and installation guide. All SOM-A255x series support this LCD kit in reference image.
- **LCD-A104-TTS1-0 (Optional item)**
  10.4" TFT SVGA LCD kit. The kit includes 10.4" TFT SVGA LCD (AUO/ G104SN03v2), 4-wires resistive T/S, inverter, cables and installation guide. Only SOM-A255F & SOM-A2552 series can support this LCD-out mode.
- **LCD-A150-TTX2-0 (Optional item)**
  15" TFT XGA LCD kit. The kit includes 15" TFT XGA LCD (AUO/ M150XN07), 4-wires resistive T/S, inverter, cables and installation guide. Only SOM-A255F & SOM-A2552 series can support this LCD-out mode.

SOM-A2558 series design-in kit(SOM-ADK2558-B00) is not included any LCD kit. If user needs LCD kit to evaluate, please order your suitable size LCD kit.

Risc CE-Builder

SOM-A255x series all support the Advantech optional RISC CE-Builder by which developers can manage the BSP for their own platform development thru a friendly users interface over the web.

RISC CE-Builder Solution is constituted by two parts: **Web Image Builder** and **CE-TUner.**

**Web Image Builder** offers developers an online image building mechanism through a friendly user interface to remotely conduct low-level software and platform customization / integration for their target application without knowing / using Microsoft Platform Builder. The image building machine links to Advantech's Board Support Package (BSP) library so developers can leverage Advantech's low-level software solution database.

CE-TUner is a powerful value-added system utility / tool suit for developers easily and simply develop, validate and upgrade their own SW platform solution. CE-Tuner helps users fine-tune their target SW image for optimized performance, verify settings, and platform tests before the production image is certified.

RISC CE-Builder is not included in Design-in kit. If you need more information about it, please contact with ae.risc@advanch.com.tw or advantech regional sales for further support.

1.12 SOM-A2558 Block diagram

SOM-A2558 series bases on Dual-Chips design concept, SoC Intel XScale PXA255 & I/O enhancement chip Advantech EVA-C210. The Block diagram is as following:
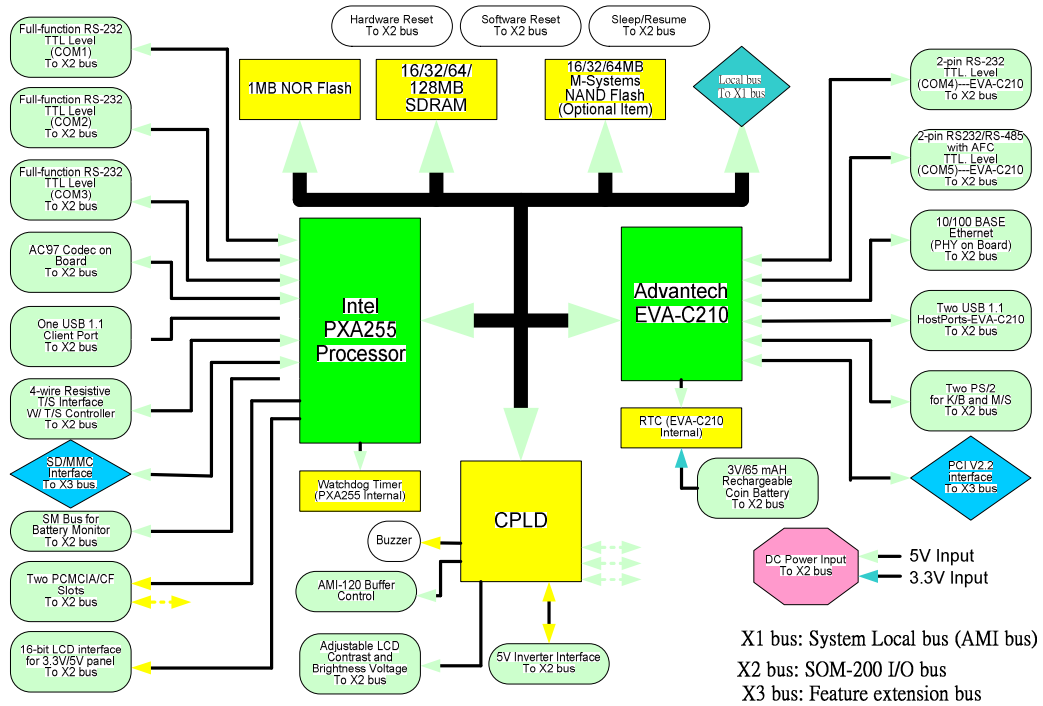
SoC Intel XScale PXA255 introduction

Intel XScale PXA255 processor is continuing the advance in handheld multimedia functionality.

PXA255 is Low power, high performance 32-bit Intel XScale® core-based CPU (200, 300 and 400 MHz). The SoC is ARM Architecture v.5TE compliant. 0.18μ process for high core speeds at low power.
Intel® Media Processing Technology including 40-bit accumulator and 16-bit SIMD to enhance audio/video decode performance.

In power field, Low Power and Turbo modes enables enhanced optimal battery life. 32 KB data and 32 KB instruction caches, 2 KB Mini data cache for streaming data.

About PXA255 I/O expansion function, Integrated Memory and PCMCIA/Compact Flash Controller with 100 MHz Memory Bus, 16-bit or 32-bit ROM/Flash/SRAM (six banks), 16-bit or 32-bit SDRAM, SMROM (four banks), as well as PCMCIA and Compact Flash for added functionality and expandability. System Control Module includes 17 dedicated general-purpose interruptible I/O ports, real-time clock, watchdog and interval timers, power management controller, interrupt controller, reset controller, and two on-chip oscillators.

Peripheral Control Module offers 16 channel configurable DMA controller, integrated LCD controller with unique DMA for fast color screen support, Bluetooth** I/F, serial ports including IrDA, I2C, I2S, AC97, three UARTs(1 Full H/W flow control), SPI and enhanced SSP, USB end point interface, and MMC/SD Card Support for expandable memory and I/O functionality.

About Intel PXA255 SoC detail information, user could visit Intel web site for more.

Enhance I/O chip Advantech EVA-C210 introduction

The Advantech EVA-C210 Companion Chip is a companion chip to the Intel® PXA255 processor based on XScale^{TM} technology. It provides a variety of functions suitable for use in a high performance computer system. The integrated on-chip functions include:

- Companion to Intel® PXA255 processor
- System Bus Interface (SBI) to AHB Wrapper
- Shared Memory Controller supports SDRAM
- Two PS/2 ports are provided for use with keyboards and mice
- Real Time Clock (RTC) with calendar function
- I^{2}C Controller
- UART Controller with auto-flow-control function for RS485
- 16550-compatible UART
- Provide up to 32 bits of General Purpose I/O (GPIO)
- Two independent 16-bit Timers
- Two ports USB Host Controllers with PHY which are compliant with

USB Spec. Rev. 1.1

- PCI Bus Controller (FPCI) which is compliant with PCI Spec. Rev. 2.2

- One port Ethernet 10/100 MAC Controller

- Interrupt Controller

- Power Management Unit with Normal, Sleep, Deep Sleep mode and Power-off mode.

- 3.3V power supply with 3V/5V tolerant

- 256 BGA package

System Memory

SOM-A2558 SDRAM can be configured as 4/8/16/32/64/128/256MB. Users can base on their requirement to reconfigure the SDRAM size.

There are two functions Flash on SOM-A2558 series. One is Boot Flash, the other is Storage Flash.

Boot Flash is 1MB NOR flash. In standard SOM-A2558 series product, Advantech will pre-install the WinCE bootloader in it.

Storage Flash is used to save image & user APs. Storage Flash size is also reconfigurable. The Storage Flash is M-system Flash. Storage Flash size could be 0/16/32/64 MB. SOM-A2558 series have Multiple boot options through the on-board Flash or Compact Flash Card (CFC) for easy maintain and cost saving. If Storage Flash is 0MB that means user should put the image in Compact Flash Card.

CPLD

SOM-A2558 series have one CPLD on board. The CPLD take charges of the following function:

- System memory assignments
- I/O control
- RTC control

Base on Advantech policy, Advantech won't release the CPLD code to user. In fact, when user designs their own target carrier board, they don't need to know the CPLD code. Advantech will release memory map of available memory block and available GPIOs. These are fully enough to users to develop their own carrier board.

10

1.2 System Specifications

The following table is SOM-A2558 series functional specifications.

SOM-A2558 standard product specification table

Model Func.	SOM-A2558-440B0	Reconfiguration Option
CPU	PXA255- 400MHz	200/300/400 MHz
I/O Enhance Chip	Advantech EVA-C210	-
Graphic Chip	PXA255 built-in	-
System Memory(SDRAM)	64MB SDRAM	16/32/64/128 MB
Boot loader Flash	1MB NOR Flash	-
On-board Flash (Image & Storage)	0MB	0/16/32/64MB
OS Image Storage	Thru CFC	-
AMI Bus(X1 bus)	100-pin B2B conn w/ buffer drive	Yes
Feature Extension Bus (X2 Bus)	100-pin B2B conn (the conn. Include PCI,ZV & SD/MMC I/F)	Yes
Watch Dog	PXA255 Built-in	-
RTC	EVA-C210 Built-in	-
System Backup battery	For RTC/SDRAM	-
Serial Port	3x Full RS-232 (TTL); 1x 2-wires RS-232 (TTL); 1x 3-wires for RS-232 or RS-485	-
Ethernet	1x 10/100 Base-T	-
PCMCIA/ Compact Flash	2 Slots PCMCIA/CF or 1xPCMCIA & 1xCF	-
USB Host	2x USB 1.1 Host	-
USB Client	1x USB 1.1 Client	-
SD/MMC	1xCh(support 1 bit memory mode)	
PS/2	2x Ch for K/B & MS	-
LCD(TTL level)	Up to VGA LCD-16-bit TFT/STN/DSTN	-
T/S	4-wire resistive	Yes
Audio Codec	AC'97 codec on board. Support Mic-in, Line-in, Line-out speaker-out	Yes
Buzzer control	Yes	-
SM Bus	Yes	-

Hardware Reset	Yes	-
Software Reset	Yes	-
Resume	Yes	-
OS support	WinCE.NET	Linux(By customer request)
Power input	3.3V/5V	-
Operating temperature	0~60	Optional for -10~60 & -20~80
Operating humidity	0%~90%	-
Certification	FCC/CE	-
Form factor	68mm*68mm*6.8mm	-

Ps.. "Reconfiguration Option" column provide users many choices. "-"means no option. If standard product SOM-A2558-440B0's spec. doesn't fit user's requirement, user could contact with Advantech for SOM-A2558 reconfiguration.

* Advantech SOM-A255x series have wide temperature products. About detail product information, user could visit website http://www.advantech.com.tw/epc/phoenix/ . User also could contact with ae.risc@advanch.com.tw or advantech regional sales for further information.

SOM-A2558-440B0 is off-the-shelf standard product. Advantech welcome SOM-A2558 re-configuration demand. Users could base on the column of SOM-A2558 spec. to re-configurate userized SOM-A2558. "Reconfiguration Option" column provide users many choices. "-"means no option. If standard product SOM-A2558-440B0's spec. doesn't fit user's requirement, user could contact with Advantech for SOM-A2558 reconfiguration.

1.2.1 Mechanical Specification

Following figure shows the mechanical drawing of SOM-A2558 series.
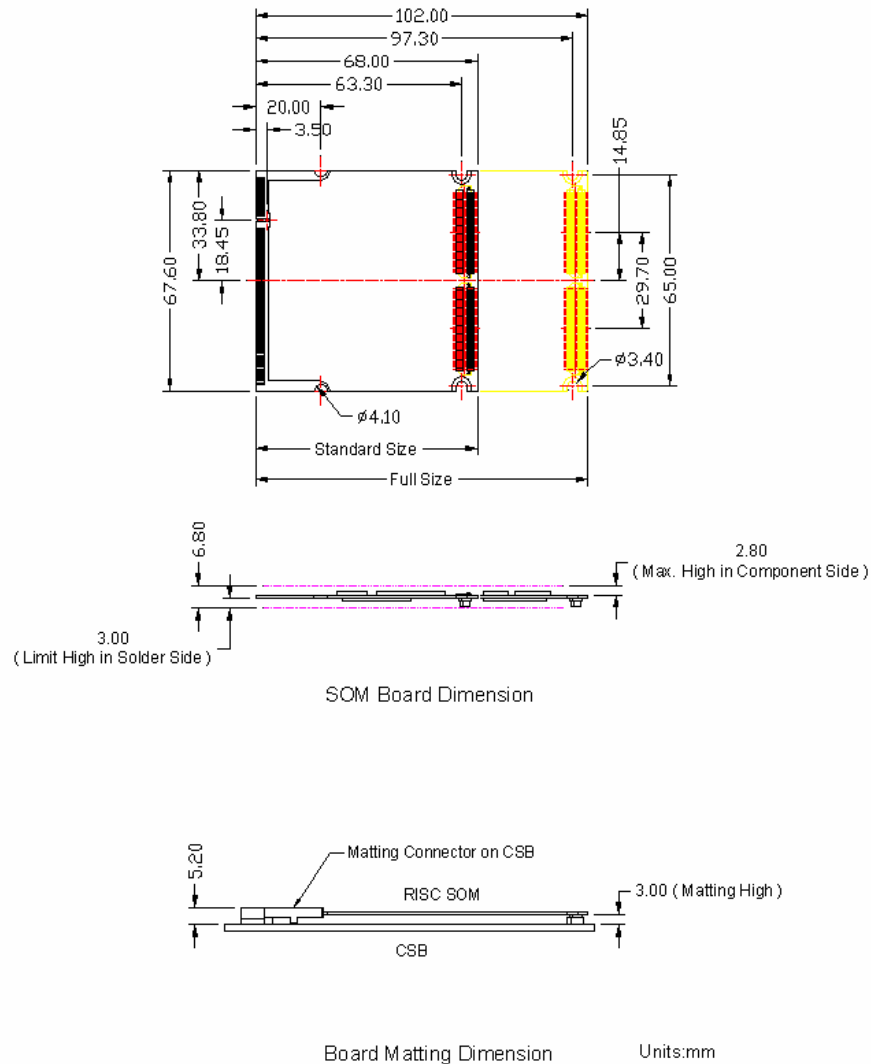
The above figure shows the SOM-A2558 mechanical drawing. Users could follow the above figure to implement the layout procedure.

1st drawing shows the SOM-A2558 module PCB mechanical data. When users enter the layout procedure, user could follow the 1st drawing to place the connector. SOM-A2558 series PCB form factor is 68mm*68mm*68mm.

The 2nd drawing shows the PCB thickness limitation. The component side height is 2.8mm, and the solder side maximum height is 3.00mm and the PCB thickness is 1.00mm.

The 3rd drawing shows allied mechanical data of SOM-A2558 series board and CSB. Users could see that the matting height is 3.00mm and the solder side maximum height of SOM-A2558 is also 3.00mm. So, **Advantech don't suggest users to place any components between SOM module and CSB in layout stage. It could be short!**

Most users will question the height of SOM structure product. Does product be too thick based on SOM structure product? User could see the

answer in the 3rd mechanical drawing. Maximum height of SOM module allied with CSB is 5.20mm. One port USB 1.1 host connector height is 8.37mm, 1 DB-9 RS-232 connector is 12.53mm, 1 type-II CF slot is 8.72mm. So, this is the answer! If users want to use any standard I/O connector on CSB, then SOM structure is not the maximum height maker. The maximum highness is decided by I/O connector, not SOM structure.

1.2.2 Power System Requirement

SOM-A2558 Operating DC value table

Symbol	Description	Min.	Typ.	Max.
SYS_VCC3P3	SOM system DC 3.3V DC-in power source	3	3.3	3.6
SYS_VCC	SOM system DC 5.0V DC-in power source	4.5	5.5	5.5
BAT_VCC	Back-up power source for RTC & SDRAM	-		SYS_VCC3P3
Input DC Operating Conditions				
VIH	Input High Voltage, all standard input and I/O pins	0.8*VCC		VCC
VIL	Input Low Voltage, all standard input and I/O pins	VSS		0.2*VCC
Output DC Operating Conditions				
VOH	Output High Voltage, all standard output and I/O pins	VCC-0.1		VCC
VOL	Output Low Voltage, all standard output and I/O pins	VSS		VSS+0.4

1.2.3 Power Consumption

In WinCE O.S. environment, SOM-A2558 series products have 3 kinds of operating model :

- Normal mode: I/O and system all work well. All components on SOM-A55x are powered.
- Idle mode: I/O and system all work well except backlight control circuit. In order to do power-saving, LCD backlight control circuit will disable the LCD backlight inverter.
- Suspend mode: all devices are no-powered except SDRAM, RTC(real time clock) & some CPU(PXA255) power pins. In suspend mode, SOM-A255x series are only powered by BAT_VCC pin (Li-ion 3.0V coin battery from CSB).If user doesn't design coin battery to power BAT_VCC pin, then Suspend mode doesn't work on SOM-A55x series products.

About detail power consumption of every SOM-A255x series, please contact with ae.risc@advantech.com.tw.

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Chapter 2 Assignments and Descriptions

2.1 Connector Locations

JP1:PXA255 Jtag conn.

X2: SODIMM-200 I/O Bus

JP2:CPLD Jtag conn.
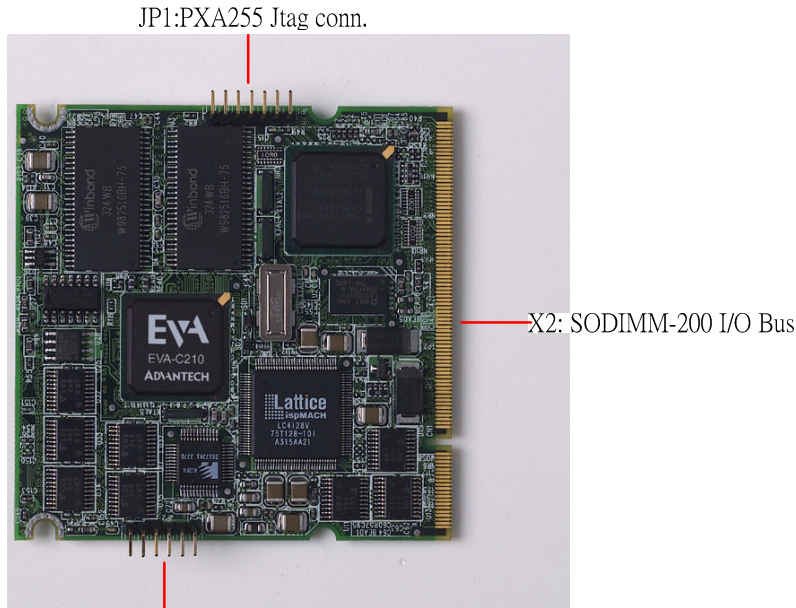
Figure SOM-A2558 series component side

JP2:CPLD Jtag conn.

X1 : AMI Bus

X2: SODIMM-200 I/O Bus

X3:Feature Ext Bus

JP1:PXA255 Jtag conn.
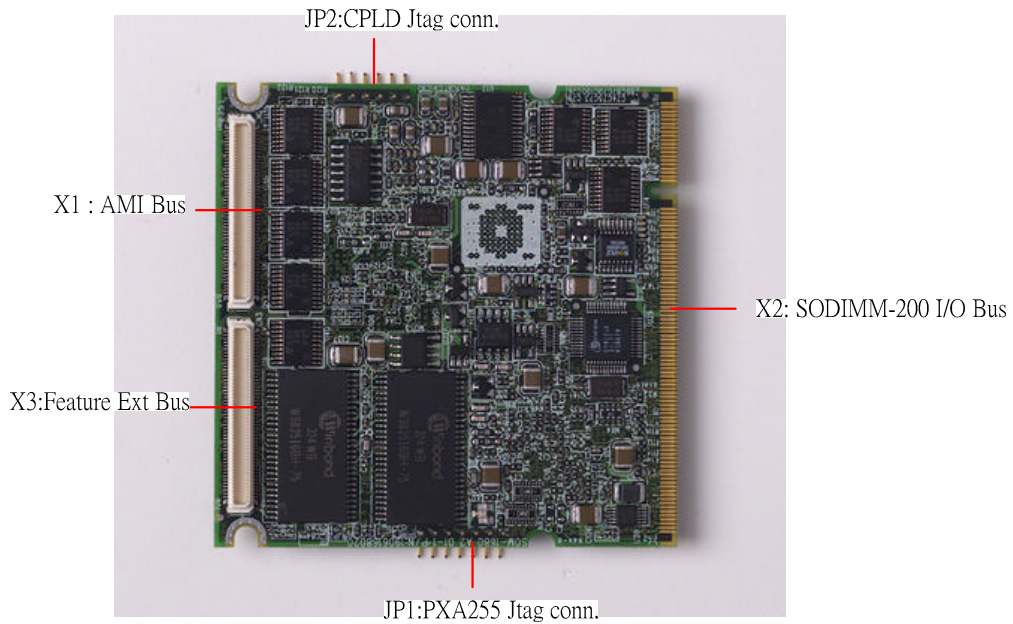
Figure SOM-A2558 series solder side

15

SOM Connector vendor table

Connector	vendor	PN
AMI bus (X1)	Matsushita electric works, LTD.	AXK600335
SOM-R200 (X2)	Standard Golden finger 200-pin	-
Feature extension bus (X3)	Matsushita electric works, LTD.	AXK600335
JP1	PXA255 JTAG pin header	-
JP2	SOM CPLD JTAG port	-

PS.JP1 & JP2 are 2.00 mm 6*1 pin-headers.

CSB Mating Connector table

Connector	vendor	PN
AMI bus (X1)	Matsushita electric works, LTD.	AXK500135
SODIMM-200 (X2)	QUASAR SYSTEM INC.	CA0075-200N31
Feature extension bus (X3)	Matsushita electric works, LTD.	AXK500135

In advantech RISC SOM-A200 ultra low power series (SOM-A2552, SOM-A2558 and SOM-A2558) all follow the same pin definition in X1,X2 and X3. So, users could design their own CSB to be compatible with all advantech RISC ultra low power series SOM easily. In this way, users' CSB will have powerful upgrade capability & option choice.

X1: AMI bus

AMI bus connector is PXA255 ARM bus. It includes complete system address lines, data lines, GPIOs (for interrupt source) and Chip select pins (nCS). Users could use this bus to extend any other IC controller on CSB to implement the function which SOM modules not provide. In order to keep the system bus signals well, every address lines and data lines are driven by buffers. Buffers' signals direction controls are implemented by CPLD.

X2: SODIMM-200 connector

Most I/O functions fog in X2. X2 includes PCMCIA/CF, T/S, Audio, system reset control, SOM system power input pins, I2C, USB host, USB client, RS-232 ports, RS-485 port, LCD out and PS/2 ports. Every I/O functions will be described in the following content in detail.

X3: Feature Extension connector

Advantech SOM-A200 series products use dual-chip or triple-chip design concepts. The companion chip's I/O function will come out through the X3. In SOM-A2558 series, PCI, SD/MMC I/F is included in X3.

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RECD SOM is a powerful and helpful architecture for internal or users use to implement a RISC system. There are three types of interfaces. One is SO-DIMM 200 gold finger interface and two 100-pin B2B connectors.

Pin Definition
¦ JP1   PXA255 JTAG pin header

Pin Num.	Description	Note
1	TCK	
2	TDI	
3	TDO	
4	TMS	
5	nJTAGTRST	
6	GND	
7	nRESET	

Pin type
P : DC power pin or system ground pin
I : digital input pin
O : digital output pin
IO : bidirectional pin
AI : analog input pin
AO : analog output pin
- : no function

¦ SODIMM-200 Pin Out Table (X2)

Pin No.	Signals	Type	Description	Default state
1	SA_SKT_D0	AIO	PCMCIA/CF data 0	No pulling
2	SA_SKT_D8	IO	PCMCIA/CF data 8	No pulling
3	SA_SKT_D1	IO	PCMCIA/CF data 1	No pulling
4	SA_SKT_D9	IO	PCMCIA/CF data 9	No pulling
5	SA_SKT_D2	IO	PCMCIA/CF data 2	No pulling
6	SA_SKT_D10	IO	PCMCIA/CF data 10	No pulling
7	SA_SKT_D3	IO	PCMCIA/CF data 3	No pulling
8	SA_SKT_D11	IO	PCMCIA/CF data 11	No pulling
9	SA_SKT_D4	IO	PCMCIA/CF data 4	No pulling
10	SA_SKT_D12	IO	PCMCIA/CF data 12	No pulling
11	SA_SKT_D5	IO	PCMCIA/CF data 5	No pulling
12	SA_SKT_D13	IO	PCMCIA/CF data 13	No pulling
13	SA_SKT_D6	IO	PCMCIA/CF data 6	No pulling
14	SA_SKT_D14	IO	PCMCIA/CF data 14	No pulling
15	SA_SKT_D7	IO	PCMCIA/CF data 7	No pulling
16	SA_SKT_D15	IO	PCMCIA/CF data 15	No pulling
17	SA_SKT_A14	IO	PCMCIA/CF address 14	No pulling

RISC Express

18	**SA_SKT_A15**	IO	PCMCIA/CF address 15	No pulling
19	**SA_SKT_A12**	IO	PCMCIA/CF address 12	No pulling
20	**SA_SKT_A13**	IO	PCMCIA/CF address 13	No pulling
21	**SA_SKT_A10**	IO	PCMCIA/CF address 10	No pulling
22	**SA_SKT_A11**	IO	PCMCIA/CF address 11	No pulling
23	**SA_SKT_A8**	IO	PCMCIA/CF address 8	No pulling
24	**SA_SKT_A9**	IO	PCMCIA/CF address 9	No pulling
25	**SA_SKT_A6**	IO	PCMCIA/CF address 6	No pulling
26	**SA_SKT_A7**	IO	PCMCIA/CF address 7	No pulling
27	**SA_SKT_A4**	IO	PCMCIA/CF address 4	No pulling
28	**SA_SKT_A5**	IO	PCMCIA/CF address 5	No pulling
29	**SA_SKT_A2**	IO	PCMCIA/CF address 2	No pulling
30	**SA_SKT_A3**	IO	PCMCIA/CF address 3	No pulling
31	**SA_SKT_A0**	IO	PCMCIA/CF address 0	No pulling
32	**SA_SKT_A1**	IO	PCMCIA/CF address 1	No pulling
33	**SA_SKT_A16**	IO	PCMCIA/CF address 16	No pulling
34	**SA_SKT_A17**	IO	PCMCIA/CF address 17	No pulling
35	**SA_SKT_A18**	IO	PCMCIA/CF address 18	No pulling
36	**SA_SKT_A19**	IO	PCMCIA/CF address 19	No pulling
37	**SA_SKT_A20**	IO	PCMCIA/CF address 20	No pulling
38	**SA_SKT_A21**	IO	PCMCIA/CF address 21	No pulling
39	**SA_SKT_A22**	IO	PCMCIA/CF address 22	No pulling
40	**nSA_SKT_IOR**	O	PCMCIA I/O read. Performs read transactions from PCMCIA I/O space.	No pulling
41	**SA_SKT_A24**	IO	PCMCIA/CF address 24	No pulling
42	**XP**	AI	4-wires resistive touch screen signals: X+ Position Input.	No pulling
43	**nSA_SKT_WE**	O	PCMCIA write enable. (output) Performs writes to PCMCIA memory and to PCMCIA attribute space. Also used as the write enable signal for Variable Latency I/O.	No pulling
44	**YP**	AI	4-wires resistive touch screen signals: Y+ Position Input.	No pulling
45	**nSA_SKT_IOW**	O	PCMCIA I/O write signal. (output) Performs write transactions to PCMCIA I/O space.	No pulling
46	**XN**	AI	4-wires resistive touch screen signals: X– Position Input	No pulling
47	**nSA_SKT_RE G**	O	PCMCIA Register select. (output) Indicates that the target address on a memory transaction is attribute space. Has the same timing as the address bus.	No pulling
48	**YN**	AI	4-wires resistive touch screen signals: Y– Position Input	No pulling
49	**SA_SKT_A23**	IO	PCMCIA/CF address 23	No pulling

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50	GND	P	Ground	-
51	SA_SKT_A25	IO	PCMCIA/CF address 25	No pulling
52	AC97_EAPD	O	External audio Amplifier power down control	No pulling
53	nSA_SKT_OE	O	PCMCIA output enable. (output) Reads from PCMCIA memory and to PCMCIA attribute space.	No pulling
54	LINEOUT_R	AO	Audio line-Out right channel	-
55	nSA_SKT1_CD 1	I	PCMCIA/CF slot 0 card detect pin	No pulling
56	LINEOUT_L	AO	Audio line-Out left channel	-
57	nSA_SKT0_CD 1	I	PCMCIA/CF slot 1 card detect pin 1.	No pulling
58	AC97_LINEIN_ R	AI	Audio line input right channel.	-
59	nSA_SKT1_CE 1	O	PCMCIA/CF slot 0 card enable pin 1.	No pulling
60	AC97_LINEIN_ L	AI	Audio line input left channel.	-
61	nSA_SKT0_CE 1	O	PCMCIA/CF slot 0 card enable pin 1.	No pulling
62	MIC_IN	AI	First Microphone input	-
63	nSA_SKT1_CE 2	O	PCMCIA/CF slot 1 card enable pin 2.	No pulling
64	GND	P	Ground	-
65	SA_SKT1_VCC	P	PCMCIA/CF slot 1 power pin	-
66	nSA_SKT0_VS 1	I	PCMCIA/CF slot 0 voltage sense pin 1.	Pull high with 10Kohm
67	nSA_SKT1_VS 1	I	PCMCIA/CF slot 1 voltage sense pin 1.	Pull high with 10Kohm
68	nSA_SKT0_CE 2	O	PCMCIA/CF slot 0 card enable pin 2.	No pulling
69	SA_SKT1_RDY	I	PCMCIA/CF slot 1 ready pin.	Pull high with 10Kohm
70	SA_SKT0_RDY	I	PCMCIA/CF slot 0 ready pin.	Pull high with 10Kohm
71	nSA_SKT0_VS 2	I	PCMCIA/CF slot 0 voltage sense pin 2.	Pull high with 10Kohm
72	nSA_SKT1_VS 2	I	PCMCIA/CF slot 1 voltage sense pin 2.	Pull high with 10Kohm
73	SA_SKT0_RST	O	PCMCIA/CF slot 0 reset pin.	Pull high with 10Kohm
74	SA_SKT1_RST	O	PCMCIA/CF slot 1 reset pin.	Pull high with 10Kohm
75	nSA_SKT0_W AIT	I	PCMCIA/CF slot 0 wait signals. Driven low by the PCMCIA card to extend the length of the transfers to/from the PXA255 processor.	Pull high with 10Kohm
76	nSA_SKT1_CD	I	PCMCIA/CF slot 1 card detect pin	No pulling

	2		2.	
77	nSA_SKT1_WAIT	I	PCMCIA/CF slot 1 wait signals. Driven low by the PCMCIA card to extend the length of the transfers to/from the PXA255 processor.	Pull high with 10Kohm
78	nSA_SKT0_CD2	I	PCMCIA/CF slot 0 card detect pin 2.	No pulling
79	nSA_SKT0_IOIS16	I	IO Select 16. (input) Acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address.	Pull high with 10Kohm
80	SA_SKT0_VCC	P	PCMCIA/CF slot 0 power pin.	Powered
81	nSA_SKT1_IOIS16	I	PCMCIA/CF slot 0 IO Select 16. Acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address.	Pull high with 10Kohm
82	nSA_PWR_ON	I	System suspend/wakeup input pin. Falling edge triggered.	Pull high with 10Kohm
83	nBATT_FALT	I	Main Battery Fault. Signals that main battery is low or removed. Assertion causes PXA255 processor to enter sleep mode or force an Imprecise Data Exception, which cannot be masked. PXA255 processor will not recognize a wakeup event while this signal is asserted. Minimum assertion time for nBATT_FAULT is 1 ms.	Pull high with 100Kohm
84	nSW_RESET	I	System software reset input pin. Falling edge triggered.	Pull high with 10Kohm
85	nVDD_FALT	I	VDD Fault. Signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA255 processor to enter sleep mode or force an Imprecise Data Exception, which cannot be masked. nVDD_FAULT is ignored after a wakeup event until the power supply timer completes (approximately 10 ms). Minimum assertion time for nVDD_FAULT is 1 ms.	Pull high with 100Kohm
86	nRESET_OUT	O	Reset Out. Asserted when nRESET is asserted and deasserts after nRESET is deasserted but before the first instruction fetch. nRESET_OUT is also asserted for "soft" reset events: sleep, watchdog reset, or GPIO reset.	No pulling
87	GND	P	Ground	-

20

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88	PWR_EN	O	Power Enable for the power supply. (output) When negated, it signals the power supply to remove power to the core because the system is entering sleep mode.	Pull high with 100Kohm
89	BAT_VCC	P	3.0V li-ion coin battery positive pole input pin.	No pulling
90	nRESET	I	System hardware reset input pin. Falling edge triggered. Hard reset. (input) Level sensitive input used to start the processor from a known address. Assertion causes the current instruction to terminate abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable and the internal 3.6864 MHz oscillator has stabilized.	Pull high with 10Kohm
91	nDC_IN	I	System DC input indicator pin. When the pin is low, it means system is powered by external DC power source. If user target device is not power by battery, use could use this pin as GPIO. The pin connects to SoC PXA255 GPIO16.	Pull low with 1Kohm
92	SYS_VCC	P	SOM system DC power 5V input pin. SYS_VCC should always be powered by DC 5V even in sleep mode.	-
93	SYS_VCC3P3	P	SOM system DC power 3.3V input pin. SYS_VCC should always be powered by DC 3.3V even in sleep mode.	-
94	SYS_VCC	P	SOM system DC power 5V input pin. SYS_VCC should always be powered by DC 5V even in sleep mode.	-
95	SYS_VCC3P3	P	SOM system DC power 3.3V input pin. SYS_VCC should always be powered by DC 3.3V even in sleep mode.	-
96	SMBUS_CLK	IO	System Management Bus clock pin. The pin is implemented by SoC PXA255 I2C bus.	Pull high with 4.7Kohm
97	SYS_VCC3P3	P	SOM system DC power 3.3V input pin. SYS_VCC should always be powered by DC 3.3V even in sleep mode.	-

98	SMBUS_DAT	IO	System Management Bus data pin. The pin is implemented by SoC PXA255 I2C bus.	Pull high with 4.7Kohm
99	SYS_VCC3P3	P	SOM system DC power 3.3V input pin. SYS_VCC should always be powered by DC 3.3V even in sleep mode.	-
100	USB_CP	IO	USB Client Positive pin	No pulling
101	SYS_VCC3P3	P	SOM system DC power 3.3V input pin. SYS_VCC should always be powered by DC 3.3V even in sleep mode.	Powered
102	USB_CN	IO	USB Client Negative pin.	No pulling
103	SYS_VCC3P3	P	SOM system DC power 3.3V input pin. SYS_VCC should always be powered by DC 3.3V even in sleep mode.	-
104	BUZZER_OUT	O	Buzzer-out control signals. User can use the pin to control buzzer power pin.	No pulling
105	USB_LINK_5V	I	USB client link status indicator pin. When the pin is high, it means USB client port has been plugged-in USB device.	Pull low with 100Kohm
106	UART2_RTS	O	UART2 Request-to-Send signal pin. If user doesn't need UART2 function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO45.	Pull high with 100Kohm
107	GND	P	Ground	-
108	UART2_DCD	I	UART2 data-Carrier-Detect signal pin.	Pull high with 100Kohm
109	UART3_DCD	I	UART3 data-Carrier-Detect signal pin.	Pull high with 100Kohm
110	UART2_DSR	I	UART2 Data-Set-Ready signal pin.	Pull high with 100Kohm
111	UART3_DSR	I	UART3 Data-Set-Ready signal pin.	Pull high with 100Kohm
112	UART2_TXD	O	UART2 Transmit signal pin. If user doesn't need UART2 function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO43.	Pull high with 100Kohm
113	UART3_RXD	I	UART3 Receive signal pin. If user doesn't need UART3 function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO46.	Pull high with 100Kohm
114	UART2_RXD	I	UART2 Receive signal pin. If user	Pull high with

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			doesn't need UART2 function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO42.	100Kohm
115	UART3_RTS	O	UART3 Request-to-Send signal pin.	Pull high with 100Kohm
116	UART2_CTS	I	UART2 Clear-to-Send signal pin. If user doesn't need UART2 function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO44.	Pull high with 100Kohm
117	UART3_TXD	O	UART3 Transmit signal pin. If user doesn't need UART3 function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO47.	Pull high with 100Kohm
118	UART2_DTR	O	UART Data-Terminal-Ready signal pin.	Pull high with 100Kohm
119	UART3_CTS	I	UART3 Clear-to-Send signal pin.	Pull high with 100Kohm
120	UART2_RI	I	UART2 Ring Indicator signal pin.	Pull high with 100Kohm
121	UART3_DTR	O	UART3 Data-Terminal-Ready signal pin.	Pull high with 100Kohm
122	UART3_RI	I	UART3 Ring Indicator signal pin.	Pull high with 100Kohm
123	UART1_DSR	I	UART1 Data-Set-Ready signal pin.	Pull high with 100Kohm
124	UART1_DCD	I	UART1 Data-Carrier-Detect signal pin.	Pull high with 100Kohm
125	UART1_CTS	I	UART1 Clear-to-Send signal pin.	Pull high with 100Kohm
126	UART1_RXD	I	UART1 Receive signal pin.	Pull high with 100Kohm
127	UART1_RTS	O	UART1 Request-to-Send signal pin.	Pull high with 100Kohm
128	UART1_TXD	O	UART1 Transmit signal pin.	Pull high with 100Kohm
129	UART1_DTR	O	UART1 Data-Terminal-Ready signal pin.	Pull high with 100Kohm
130	GND	P	Ground	-
131	UART1_RI	I	UART Ring Indicator signal pin.	Pull high with 100Kohm
132	TX-	O	10/100 BASE-T transmit Data negative pin.	No pulling
133	nLINK_LED	O	Link LED & Activity LED. Active states indicate the good link for 10Mbps and 100Mbps operations. It is also an active LED	Pull high with 10Kohm

RISC Express

23

			function when transmitting or receiving data. Active states see LED configuration OP2: (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9161 according to the Table A. The value is latched into the DM9161 registers at power-up/reset	
134	TX+	O	10/100 BASE-T transmit Data positive pin.	No pulling
135	nSPEED_LED	O	Speed LED. Active states indicate the 100Mbps mode. Active states see LED configuration When bit 6 of Register 16 is set high, it controls the SPEED LED as 100Base-TX SD signal output. For debug only OP1: (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9161 according to the Table A. The value is latched into the DM9161 registers at power-up/reset	Pull high with 10Kohm
136	GND	P	Ground	-
137	VDD_ENA	O	LCD power control signal. User can use this pin to control the LCD logic power MOS switch to achieve power-saving.	No pulling
138	RX-	I	10/100 BASE-T receive data negative pin.	No pulling
139	VEE_ENA	O	STN LCD VEE power control signal. User can use this pin to control STN LCD VEE power MOS switch to achieve power-saving.	No pulling
140	RX+	I	10/100 BASE-T receive data negative pin.	No pulling
141	VBK_ENA	O	LCD back light inverter power control signal. User can use this pin to control the LCD backlight inverter to achieve power-saving.	No pulling
142	USB_N1	IO	USB host port1 D- data line.	No pulling
143	USB_N2	IO	USB host port2 D- data line.	No pulling
144	USB_P1	IO	USB host port1 D+ data line.	No pulling
145	USB_P2	IO	USB host port2 D+ data line.	No pulling
146	N.C.	-	N.C. just float this pin.	-
147	N.C.	-	N.C. just float this pin.	-
148	UART5_RXD	I	UART5 Receive signal pin.	Pull high with 100Kohm

149	UART4_RXD	I	UART5 Receive signal pin.	Pull high with 100Kohm
150	UART5_RTS	O	UART5 Data-Terminal-Ready signal pin.	Pull high with 100Kohm
151	UART4_TXD	O	UART4 Transmit signal pin.	Pull high with 100Kohm
152	UART5_TXD	O	UART5 Transmit signal pin.	Pull high with 100Kohm
153	MSCLK	IO	PS/2 mouse clock	Pull high with 10Kohm
154	KBDATA	IO	PS/2 keyboard data	Pull high with 10Kohm
155	MSDATA	IO	PS/2 mouse data	Pull high with 10Kohm
156	KBCLK	IO	PS/2 keyboard clock	Pull high with 10Kohm
157	nVBRIR_INC	O	One of LCD inverter backlight brightness control signals. nVBRIR_INC is used to increase or decrease Wiper Control. Advantech suggests to connect the pin to DS1804 1st pin.	No pulling
158	N.C.	-	N.C. just float this pin.	-
159	nVBRIR_UnD	O	One of LCD inverter backlight brightness control signals. nVBRIR_UnD is used be Up/Down Control. Advantech suggests to connect the pin to DS1804 2nd pin.	No pulling
160	N.C.	-	N.C. just float this pin.	-
161	VBRIR_CS	O	One of LCD inverter backlight brightness control signals. VBRIR_CS is used be chip select pin. Advantech suggests to connect the pin to DS1804 7th pin.	No pulling
162	N.C.	-	N.C. just float this pin.	-
163	nVCONR_INC	O	One of STN LCD contrast control signals. nVCONR_INC is used be increase/decrease Wiper Control pin. Advantech suggests to connect the pin to DS1804 1st pin.	No pulling
164	N.C.	-	N.C. just float this pin.	-
165	VCONR_CS	O	One of STN LCD contrast control signals. VCONR_CS is used be chip select pin. Advantech suggests to connect the pin to DS1804 7th pin.	No pulling
166	N.C.	-	N.C. just float this pin.	-
167	VCONR_UnD	O	One of STN LCD contrast control signals. VCONR_UnD is used be	No pulling

25

			Up/Down Control. Advantech suggests to connect the pin to DS1804 2nd pin.	
168	**CRT_SDA**	-	Reserved for future use. User can connect the pin to CRT I2C data pin or just float it.	Pull high with 4.71Kohm
169	**CRT_CLK**	-	Reserved for future use. User can connect the pin to CRT I2C clock pin or just float it.	Pull high with 4.71Kohm
170	**B0**	O	B0 in 24-bit TFT mode.	No pulling
171	**B1**	O	B in 24-bit TFT mode.	No pulling
172	**B2**	O	B in 24-bit TFT mode.	No pulling
173	**B3**	O	B in 24-bit TFT mode.	No pulling
174	**B4**	O	B in 24-bit TFT mode.	No pulling
175	**B5**	O	B in 24-bit TFT mode.	No pulling
176	**B6**	O	B in 24-bit TFT mode.	No pulling
177	**B7**	O	B in 24-bit TFT mode.	No pulling
178	**G0**	O	G in 24-bit TFT mode.	No pulling
179	**G1**	O	G in 24-bit TFT mode.	No pulling
180	**G2**	O	G in 24-bit TFT mode.	No pulling
181	**G3**	O	G in 24-bit TFT mode.	No pulling
182	**G4**	O	G in 24-bit TFT mode.	No pulling
183	**G5**	O	G in 24-bit TFT mode.	No pulling
184	**G6**	O	G in 24-bit TFT mode.	No pulling
185	**G7**	O	G in 24-bit TFT mode.	No pulling
186	**R0**	O	R in 24-bit TFT mode.	No pulling
187	**R1**	O	R in 24-bit TFT mode.	No pulling
188	**R2**	O	R in 24-bit TFT mode.	No pulling
189	**R3**	O	R in 24-bit TFT mode.	No pulling
190	**R4**	O	R in 24-bit TFT mode.	No pulling
191	**R5**	O	R in 24-bit TFT mode.	No pulling
192	**R6**	O	R in 24-bit TFT mode.	No pulling
193	**R7**	O	R in 24-bit TFT mode.	No pulling
194	**N.C.**	-	N.C. just float this pin.	-
195	**N.C.**	-	N.C. just float this pin.	-
196	**FLM_VSYNC**	O	Flat Panel TFT Vertical Sync/STN Frame Pulse. For TFT displays, this output connects to the Vertical Sync input of the LCD panel. For STN displays, this output connects to the Frame Clock input of the LCD panel. This output indicates the start of a new frame of pixels. The panel needs to reset its line pointers to the top of the screen.	No pulling
197	**LP_HSYNC**	O	Flat Panel TFT Vertical Sync/STN Frame Pulse. For TFT displays, this output connects to the Vertical	No pulling

26

Pin No.	Signals	Type	Description	Default state
			Sync input of the LCD panel. For STN displays, this output connects to the Frame Clock input of the LCD panel. This output indicates the start of a new frame of pixels. The panel needs to reset its line pointers to the top of the screen.	
198	**GND**	P	Ground	-
199	**M_DE**	O	Flat Panel Display Enable. This signal is used as a data enable when the pixel clock needs to latch pixel data.	No pulling
200	**SHCLK**	O	Flat Panel Pixel Clock. The active edge of FPCLK is programmable. The LCD panel uses this clock when loading pixel data into its Line Shift register. This signal connects to the TXCLK input of the LVDS transmitter.	No pulling

¦ 100-pin B2B connector Pin Out Table (X1 connector, For AMI interface)

Pin No.	Signals	Type	Description	Default state
B1	nBUF_CS2	O	**Static chip selects.** Chip selects to static memory devices such as ROM and Flash. Individually programmable in the memory configuration registers. This pin can be used with variable latency I/O devices. nBUF_CS2 directly connect to SoC PXA255 nCS2. User could use this pin as chip select pin to control the solution IC on carrier board. This pin is reserved for user to use.	Pull-high with 100K ohm
A1	ADDR15	O	SoC PXA255 system address 15	No pulling
B2	ADDR14	O	SoC PXA255 system address 14	No pulling
A2	ADDR13	O	SoC PXA255 system address 13	No pulling
B3	ADDR12	O	SoC PXA255 system address 12	No pulling
A3	ADDR11	O	SoC PXA255 system address 11	No pulling
B4	ADDR10	O	SoC PXA255 system address 10	No pulling
A4	ADDR9	O	SoC PXA255 system address 9	No pulling
B5	ADDR8	O	SoC PXA255 system address 8	No pulling
A5	ADDR24	O	SoC PXA255 system address 24	No pulling
B6	ADDR25	O	SoC PXA255 system address 25	No pulling
A6	nBUF_OE	O	Memory output enable pin. Connect	No pulling

			to the output enables of memory devices to control data bus drivers.	
B7	ADDR20	O	SoC PXA255 system address 20	No pulling
A7	nBUF_WE	O	Memory write enable. Connect to the write enables of memory devices.	No pulling
B8	ADDR22	O	SoC PXA255 system address 22	No pulling
A8	BUF_RD_nWR	O	Read/Write for static interface. Signals that the current transaction is a read or write.	No pulling
B9	GND	P	Ground	-
A9	BUF_RDY	I	Variable Latency I/O Ready pin. Notifies the memory controller when an external bus device is ready to transfer data.	Pull high with 100Kohm
B10	DATA15	IO	SoC PXA255 system data 15	No pulling
A10	DATA14	IO	SoC PXA255 system data 14	No pulling
B11	DATA13	IO	SoC PXA255 system data 13	No pulling
A11	DATA12	IO	SoC PXA255 system data 12	No pulling
B12	DATA11	IO	SoC PXA255 system data 11	No pulling
A12	DATA10	IO	SoC PXA255 system data 10	No pulling
B13	DATA9	IO	SoC PXA255 system data 9	No pulling
A13	DATA8	IO	SoC PXA255 system data 8	No pulling
B14	DATA31	IO	SoC PXA255 system data 31	No pulling
A14	DATA30	IO	SoC PXA255 system data 30	No pulling
B15	DATA29	IO	SoC PXA255 system data 29	No pulling
A15	DATA28	IO	SoC PXA255 system data 28	No pulling
B16	DATA27	IO	SoC PXA255 system data 27	No pulling
A16	DATA26	IO	SoC PXA255 system data 26	No pulling
B17	DATA25	IO	SoC PXA255 system data 25	No pulling
A17	DATA24	IO	SoC PXA255 system data 24	No pulling
B18	nBUF_SDRAS	O	SDRAM RAS. Connect to the row address strobe (RAS) pins for all banks of SDRAM.	No pulling
A18	nBUF_SDCS0	O	SDRAM CS for bank 0. Connect to the chip select (CS) pin for SDRAM. For the PXA255 processor nBUF_SDCS0 can be Hi-Z.	No pulling
B19	BUF_DQM0	O	SDRAM DQM for data byte 0. Connect to the data output mask enables (DQM) for SDRAM.	No pulling
A19	BUF_DQM2	O	SDRAM DQM for data byte 2. Connect to the data output mask enables (DQM) for SDRAM.	No pulling
B20	BUF_DQM3	O	SDRAM DQM for data byte 3. Connect to the data output mask enables (DQM) for SDRAM.	No pulling
A20	nBUF_PWAIT	I	PCMCIA wait. (input) Driven low by the PCMCIA card to extend the	Pull high with

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			length of the transfers to/from the PXA255 processor.	100Kohm
B21	BUF_SDCLK1	O	**SDRAM Clock 1.** Connect SDCLK [1] to the clock pins of SDRAM in bank pairs 0/1. They are driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide by 2 clock speed and may be turned off via free running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[2:1] control register assertion bits are always deasserted upon reset.	No pulling
A21	BUF_SDCKE1	O	SDRAM and/or Synchronous Static Memory clock enable. Connect to the clock enable pins of SDRAM. It is deasserted during sleep. BUF_SDCKE1 is always deasserted upon reset. The memory controller provides control register bits for deassertion.	No pulling (For SOM-255F is BUF_SDCKE1)
B22	GND	P	Ground	-
A22	ADDR0	O	SoC PXA255 system address 0	No pulling
B23	ADDR1	O	SoC PXA255 system address 1	No pulling
A23	ADDR2	O	SoC PXA255 system address 2	No pulling
B24	ADDR3	O	SoC PXA255 system address 3	No pulling
A24	ADDR4	O	SoC PXA255 system address 4	No pulling
B25	ADDR5	O	SoC PXA255 system address 5	No pulling
A25	ADDR6	O	SoC PXA255 system address 6	No pulling
B26	ADDR7	O	SoC PXA255 system address 7	No pulling
A26	ADDR16	O	SoC PXA255 system address 16	No pulling
B27	ADDR17	O	SoC PXA255 system address 17	No pulling
A27	ADDR18	O	SoC PXA255 system address 18	No pulling
B28	ADDR19	O	SoC PXA255 system address 19	No pulling
A28	ADDR21	O	SoC PXA255 system address 21	No pulling
B29	ADDR23	O	SoC PXA255 system address 23	No pulling
A29	DATA0	IO	SoC PXA255 system data 0	No pulling
B30	DATA1	IO	SoC PXA255 system data 1	No pulling
A30	DATA2	IO	SoC PXA255 system data 2	No pulling
B31	DATA3	IO	SoC PXA255 system data 3	No pulling
A31	DATA4	IO	SoC PXA255 system data 4	No pulling
B32	DATA5	IO	SoC PXA255 system data 5	No pulling
A32	DATA6	IO	SoC PXA255 system data 6	No pulling
B33	DATA7	IO	SoC PXA255 system data 7	No pulling

29

A33	DATA16	IO	SoC PXA255 system data 16	No pulling
B34	DATA17	IO	SoC PXA255 system data 17	No pulling
A34	DATA18	IO	SoC PXA255 system data 18	No pulling
B35	DATA19	IO	SoC PXA255 system data 19	No pulling
A35	DATA20	IO	SoC PXA255 system data 20	No pulling
B36	DATA21	IO	SoC PXA255 system data 21	No pulling
A36	DATA22	IO	SoC PXA255 system data 22	No pulling
B37	DATA23	IO	SoC PXA255 system data 23	No pulling
A37	nBUF_SDCAS	O	SDRAM CAS. Connect to the column address strobe (CAS) pins for all banks of SDRAM.	No pulling
B38	nBUF_SDCS2	O	SDRAM CS for banks 2. Connect to the chip select (CS) pins for SDRAM. For the PXA255 processor nSDCS0 can be Hi-Z, Nsdcs1-3 cannot.	No pulling
A38	BUF_DQM1	O	SDRAM DQM for data bytes 1. Connect to the data output mask enables (DQM) for SDRAM.	No pulling
B39	BUF_SDCLK2	O	**SDRAM Clock 2.** Connect BUF_SDCLK[2] to the clock pins of SDRAM in bank pairs 2/3. They are driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide by 2 clock speed and may be turned off via free running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[2:1] control register assertion bits are always deasserted upon reset.	No pulling
A39	nBUF_IOIS16	I	IO Select 16. Acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address.	Pull high with 100Kohm
B40	nBUF_PWE	O	PCMCIA write enable. Performs writes to PCMCIA memory and to PCMCIA attribute space. Also used as the write enable signal for Variable Latency I/O.	No pulling
A40	KEYPAD_IRQ	I	GPIO pin. Advantech default function is used as matrix Keypad IRQ. The pin directly connects to PXA255 GPIO2 (L13 pin). If user doesn't use the matrix key pad	No pulling

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			function, use can use this pin as GPIO pin.	
B41	DISPLAY_IRQ	-	Advantech use this pin to control display chip as IRQ function. The pin is not available for CSB design of SOM-A2552 & SOM-A255F platform. SOM-A2552 & SOM-A255F user must float this pin. This pin is directly connected to SoC PXA255 GPIO3(K14).	-
A41	PXA_GP7	IO	GPIO pin. The pin directly connects to PXA255 GPIO7 (G15 pin). This GPIO pin is available for user to use.	No pulling (For SOM-255F is PXA_GPIO7)
B42	N.C.	-	N.C. just float this pin.	-
A42	C950_485_IRQ	I	Advantech default function is used as external 16C950 solution IC IRQ. The pin directly connects to PXA255 GPIO10 (F7 pin). If user doesn't design 16C950 on CSB to expand COM function, user could use this pin as GPIO.	No pulling
B43	LAN1_IRQ	I	Advantech default function is used as external LAN solution IC IRQ. The pin directly connects to PXA255 GPIO17 (D12 pin). If user doesn't design the other LAN chip on CSB to expand LAN function, user could use this pin as GPIO.	No pulling
A43	USB_IRQ	I	Advantech default function is used as external USB host solution IC IRQ. The pin directly connects to PXA255 GPIO27 (B9 pin). If user doesn't design the other USB solution chip on CSB to expand USB host function, user could use this pin as GPIO.	No pulling
B44	C954_IRQ	I	Advantech default function is used as external 16C954 solution IC IRQ. The pin directly connects to PXA255 GPIO32 (A16 pin). If user doesn't design 16C950 on CSB to expand COM function, user could use this pin as GPIO.	No pulling
A44	PXA_GP81	IO	GPIO pin. The pin directly connects to PXA255 GPIO81 (F16 pin). This GPIO pin is available for user to use.	No pulling
B45	PXA_GP82	IO	GPIO pin. The pin directly connects	No pulling

			to PXA255 GPIO82 (E16 pin). This GPIO pin is available for user to use.	
A45	PXA_GP83	IO	GPIO pin. The pin directly connects to PXA255 GPIO83 (E15 pin). This GPIO pin is available for user to use.	No pulling
B46	PXA_GP84	IO	GPIO pin. The pin directly connects to PXA255 GPIO84 (D16 pin). This GPIO pin is available for user to use.	No pulling
A46	nBUF_CS1	O	Static chip selects. Chip selects to static memory devices such as ROM and Flash. Individually programmable in the memory configuration registers. nBUF_CS1 can be used with variable latency I/O devices. Advantech default uses this pin as storage flash chip select pin. If no special application, Advantech strongly suggest user to open this pin in CSB.	Pull high with 100Kohm
B47	N.C.	-	N.C. just float this pin.	-
A47	nBUF_CS3	O	Static chip selects. Chip selects to static memory devices such as ROM and Flash. Individually programmable in the memory configuration registers. nBUF_CS3 can be used with variable latency I/O devices. Advantech uses the pin as I/O memory block. About detail description, please reference *"SOM-A255x series Memory and Interrupt Map"*.	Pull high with 100Kohm
B48	nBUF_CS5	O	Static chip selects. Chip selects to static memory devices such as ROM and Flash. Individually programmable in the memory configuration registers. nBUF_CS5 can be used with variable latency I/O devices. Advantech default uses the pin as display chip chip select pin. nBUF_CS4 pin is used for SM501 on SOM-A2552 & SOM-A255F series. If no special application, Advantech strongly suggest user to open this pin in CSB.	Pull high with 100Kohm
A48	DMA_REQ1	I	Channel 1 DMA Request. Notifies the DMA Controller that an external device requires a DMA transaction. If user wants to design a controller in	Pull low with 1Kohm

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			CSB with DMA mode, please check with ae.risc@advantech.com.tw first. If use doesn't want to use this pin as DMA_REQ, use could use the pin as GPIO. The pin connects to SoC PXA255 GPIO19.	
B49	MBREQ	I	Memory Controller alternate bus master request. Allows an external device to request the system bus from the Memory Controller. If user wants to design a controller in CSB with this pin function, please check with ae.risc@advantech.com.tw first. If use doesn't want to use this pin as DMA_REQ, use could use the pin as GPIO. The pin connects to SoC PXA255 GPIO14.	Pull low with 1Kohm
A49	DMA_ACK1	O	Channel 1 DMA acknowledge. Notifies an external device that it has been acknowledged the DMA controller. If user wants to design a controller in CSB with DMA mode, please check with ae.risc@advantech.com.tw first. If use doesn't want to use this pin as DMA_ACK, use could use the pin as GPIO. The pin connects to SoC PXA255 GPIO22.	No pulling
B50	MBGNT	O	Memory Controller grant. Notifies an external device that it has been granted the system bus. If user wants to design a controller in CSB with this pin function, please check with ae.risc@advantech.com.tw first. If use doesn't want to use this pin as MBGNT, use could use the pin as GPIO. The pin connects to SoC PXA255 GPIO13.	Pull low with 1Kohm
A50	3M6864	O	3.6864 MHz clock. Output from 3.6864 MHz oscillator.	No pulling

¦ **100-pin B2B connector Pin Out Table (X3 connector for PCI, ZV port, MMC interface and Misc. function)**

Pin No.	Signals	Type	Model	Default state
B1	PCIAD0	IO	PCI address/data 0	No pulling
A1	PCIAD1	IO	PCI address/data 1	No pulling

33

B2	PCIAD2	IO	PCI address/data 2	No pulling
A2	PCIAD3	IO	PCI address/data 3	No pulling
B3	PCIAD4	IO	PCI address/data 4	No pulling
A3	PCIAD5	IO	PCI address/data 5	No pulling
B4	PCIAD6	IO	PCI address/data 6	No pulling
A4	PCIAD7	IO	PCI address/data 7	No pulling
B5	nCBE0	IO	PCI bus command and bytes enable signal	No pulling
A5	PCIAD8	IO	PCI address/data 8	No pulling
B6	PCIAD9	IO	PCI address/data 9	No pulling
A6	PCIAD10	IO	PCI address/data 10	No pulling
B7	PCIAD11	IO	PCI address/data 11	No pulling
A7	nPCIRST	O	PCI bus reset signal	No pulling
B8	PCICLKO	IO	PCI bus clock output (Typical period: 31.2ns)	No pulling
A8	nCBE3	IO	PCI bus command and bytes enable signal	No pulling
B9	nINTD	I	PCI bus interrupt D	No pulling
A9	nINTC	I	PCI bus interrupt C	No pulling
B10	GND	P	Ground	-
A10	nINTB	I	PCI bus interrupt B	No pulling
B11	nINTA	I	PCI bus interrupt A	No pulling
A11	nGNT3	O	PCI bus grant signal	No pulling
B12	nREQ3	I	PCI bus request signal	No pulling
A12	nGNT2	O	PCI bus grant signal	No pulling
B13	nREQ2	I	PCI bus request signal	No pulling
A13	nGNT1	O	PCI bus grant signal	No pulling
B14	nREQ1	I	PCI bus request signal	No pulling
A14	GND	P	Ground	-
B15	PCIAD31	IO	PCI address/data 31	No pulling
A15	PCIAD30	IO	PCI address/data 30	No pulling
B16	PCIAD12	IO	PCI address/data 12	No pulling
A16	PCIAD13	IO	PCI address/data 13	No pulling
B17	PCIAD14	IO	PCI address/data 14	No pulling
A17	PCIAD15	IO	PCI address/data 15	No pulling
B18	GND	P	Ground	-
A18	nCBE1	IO	PCI bus command and bytes enable signal	No pulling
B19	PAR	IO	PCI bus parity bit	No pulling
A19	GND	P	Ground	-
B20	nSERR	IO	PCI bus system error signal	No pulling
A20	nPERR	IO	PCI bus parity error signal	No pulling
B21	nSTOP	IO	PCI bus stop signal	No pulling
A21	nDEVSEL	IO	PCI bus device select signal	No pulling
B22	nTRDY	IO	PCI bus target ready signal	No pulling
A22	nIRDY	IO	PCI bus initiator ready signal	No pulling
B23	nFRAME	IO	PCI bus cycle frame signal	No pulling
A23	nCBE2	IO	PCI bus command and bytes	No pulling

|			enable signal	
B24	PCIAD16	IO	PCI address/data 16	No pulling
A24	PCIAD17	IO	PCI address/data 17	No pulling
B25	PCIAD18	IO	PCI address/data 18	No pulling
A25	PCIAD19	IO	PCI address/data 19	No pulling
B26	PCIAD20	IO	PCI address/data 20	No pulling
A26	PCIAD21	IO	PCI address/data 21	No pulling
B27	PCIAD22	IO	PCI address/data 22	No pulling
A27	PCIAD23	IO	PCI address/data 23	No pulling
B28	PCIAD24	IO	PCI address/data 24	No pulling
A28	PCIAD25	IO	PCI address/data 25	No pulling
B29	PCIAD26	IO	PCI address/data 26	No pulling
A29	PCIAD27	IO	PCI address/data 27	No pulling
B30	PCIAD28	IO	PCI address/data 28	No pulling
A30	PCIAD29	IO	PCI address/data 29	No pulling
B31	N.C.	-	N.C. float this pin.	-
A31	N.C.	-	N.C. float this pin.	-
B32	N.C.	-	N.C. float this pin.	-
A32	N.C.	-	N.C. float this pin.	-
B33	N.C.	-	N.C. float this pin.	-
A33	N.C.	-	N.C. float this pin.	-
B34	N.C.	-	N.C. float this pin.	-
A34	N.C.	-	N.C. float this pin.	-
B35	nMMCD	I	SD/MMC interface card detect pin. If user doesn't need MMC/SD function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO12.	Pull high with 100Kohm
A35	MMCLK	O	MMC clock. Clock signal for the MMC Controller. If user doesn't need MMC/SD function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO6.	No pulling
B36	MMDAT3/ MMCCS0	O	Chip select pin for MMC controller. If user doesn't need MMC/SD function, user could use this pin as GPIO. The pin connects to SoC PXA255 GPIO8.	No pulling (For SOM-255F is MMCCS0)
A36	MMCMD	IO	Multimedia Card Command.	Pull high with 10Kohm
B37	MMDAT0	IO	Multimedia Card Data pin.	Pull high with 10Kohm (For SOM-255F is MMCDAT)
A37	N.C.	-	No connection. Just float this pin.	N.C. (For SOM-255F is Reserved)
B38	N.C.	-	No connection. Just float this pin.	N.C. (For SOM-255F is

RISC Express

				Reserved)
A38	**N.C.**	-	N.C. just float this pin.	-
B39	**N.C.**	-	N.C. just float this pin.	-
A39	**N.C.**	-	N.C. just float this pin.	-
B40	**N.C.**	-	N.C. just float this pin.	-
A40	**N.C.**	-	N.C. just float this pin.	-
B41	**N.C.**	-	N.C. just float this pin.	-
A41	**N.C.**	-	N.C. just float this pin.	-
B42	**N.C.**	-	N.C. just float this pin.	-
A42	**N.C.**	-	N.C. just float this pin.	-
B43	**N.C.**	-	N.C. just float this pin.	-
A43	**N.C.**	-	N.C. just float this pin.	-
B44	**N.C.**	-	N.C. just float this pin.	-
A44	**N.C.**	-	N.C. just float this pin.	-
B45	**N.C.**	-	N.C. just float this pin.	-
A45	**N.C.**	-	N.C. just float this pin.	-
B46	**N.C.**	-	N.C. just float this pin.	-
A46	**N.C.**	-	N.C. just float this pin.	-
B47	**N.C.**	-	N.C. just float this pin.	-
A47	**N.C.**	-	N.C. just float this pin.	-
B48	**N.C.**	-	N.C. just float this pin.	-
A48	**N.C.**	-	N.C. just float this pin.	-
B49	**N.C.**	-	N.C. just float this pin.	-
A49	**GND**	P	Ground	-
B50	**N.C.**	-	N.C. just float this pin.	-
A50	**N.C.**	-	N.C. just float this pin.	-

2.2 function description
2.2.1 System Bus

System Bus includes PXA255 address bus, data bus, memory control signals and GPIOs.

System Bus enters CSB by X1. In order to make sure that system bus signals have perfect electrical waves, System Bus signals are driven by buffers to enhance signals performance.
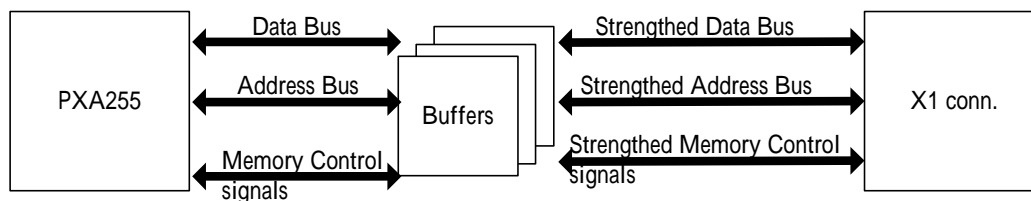
The buffers signals direction control is control by CPLD on SOM-A255x module.

2.2.2 COM

SOM-A255x series (SOM-A2552, SOM-A2558, SOM-A255F) all support 5 x RS-232 ports: 3 full function (FF) RS-232 ports, 1x 2-wire (RX, TX) RS-232 and 1x 3-wire (RX, TX, RTS) RS-232 port. COM port function assignments are as following:

- ➢ COM1: FF RS-232
- ➢ COM2: FF RS-232
- ➢ COM3: FF RS-232
- ➢ COM4: 2-wire (RX, TX) RS-232
- ➢ COM5: 3-wire (RX, TX, RTS) RS-232

All RS-232 ports are TTL levels.

According to user target CSB demand, user could define COM5 as 3-wire (RX, TX, RTS) RS-232 port or pass through RS-485 transceiver to act as RS-485 function. User could references *"Advantech SOM-A255x series CSB design guide "*to design the COM5.

2.2.3 USB 1.1 Host

SOM-A255F & SOM-A2558 series supports 2 USB host ports. SOM-A2552 series supports 1 USB host port. The USB host ports on the SOM-A255x are USB 1.1 compatible. The default Windows CE.NET and Linux on board support USB keyboards, mice and mass storage devices. User could check the " SOM-A255x series verified compatible peripherals list " to know the verified compatible peripherals. If user wants to connect other devices, it may take customization on the Windows CE.

2.2.4 USB 1.1 client

The USB client port on the SOM-A255x is USB 1.1 compatible. USB client connector is used to communicate with master device (ex: PC) for ActiveSync. About SOM-A255x series ActiveSync installation, please reference to *"Installation Guide-Advantech RISC platform with Microsoft ActiveSync 3.7".*

2.2.5 T/S

SOM-A255x series supports 4-wires (X+, X-, Y+, Y-) resistive T/S interface.

2.2.6 PCMCIA/CF

All SOM-A255x series supports 2 PCMCIA interface (I/F) or 2 CF I/F or 1 PCMCIA & 1 CF I/F. User could check " SOM-A255x Series Carrier Board Design Guide " to know how to design the I/F.

PCMCIA/CF I/F power control circuit is designed on SOM module, so PCMCIA/CF I/F is hot-swappable.

Advantech strongly suggest user to design one CF or one PCMCIA slot on user's target carrier board, even user doesn't need this port in target product. Advantech platform always use CF or PCMCIA slot to be system S/W upgrading port. If user doesn't design 1 CF or PCMCIA slot on carrier board, user will run into trouble when user wants to upgrade image, boot loader & boot-logo.

RISC Express

37

2.2.7 SD/MMC

All SOM-A255x series supports 1 slot SD/MMC port. The Multi Media Card (MMC) is a low cost data storage and communication media. The MMC controller in the SOM-A255x is compliant with *The Multi Media Card System Specification, Version 2.1*. The only exception is one and three byte data transfers are not supported.

SD/MMC I/F in SOM-A255x only support 1-bit memory mode, not support I/O mode.

2.2.8 Audio (AC'97 Codec on board)

All SOM-A255x uses Realtek ALC202 AC97 audio Codec on SOM module. SOM-A255x series provides mono microphone-in, stereo line-in, and stereo line-out interface. If users want to drive speakers, users could follow the "*Advantech SOM-A255x series CSB design guide* "to design the audio amplifier on CSB.

2.2.9 CRT-out

SOM-A255F & SOM-A2552 series supplies CRT-out I/F which resolution is up to 1024*768. CRT-out function comes from SM501. CRT-out signals are all analog signals; user must follow the analog signals layout rules.

SOM-A2558 series doesn't support CRT-out function, but user could design CRT-out solution IC on CSB to add the function on SOM-A2558 platform. About detail implement way, please check "*Advantech SOM-A255x series CSB design guide* ".

2.2.10 LCD TTL interface w/LCD Brightness & Contrast Control interface

SOM-A2552 & SOM-A255F series LCD-out interface comes from SM501. SOM-A2552 & SOM-A255F LCD-out supports 24 bit and resolution up to 1024*768. SOM-A2552 & SOM-A255F supports both active and passive LCD displays. SOM-A2558 series LCD-out function comes from SoC PXA255. SOM-A2558 LCD-out supports 16 bit and resolution up to 800*600.

The LCD signals are 3.3V level in X2. If users' CSB want to drive 5V level panel, users could design buffers on CSB to translate LCD signals level. User could refer "*Advantech SOM-A255x series CSB design guide* ".

Advantech design LCD brightness control circuit & LCD contrast control circuit on SOM-A255x series modules. STN LCD panel needs contrast control signals. In X2, LCD contrast control signals are nVCONR_INC, VCONR_CS and VCONR_UnD. The control signals are based on DALLAS DS1804 NV Trimmer Potentiometer to design. Users could check the "*Advantech SOM-A255x series CSB design guide* " to know how to wire. User could check "to know how to control.

Brightness control signals are used to control the LCD backlight inverter lamp current. In X2, LCD brightness control signals are nVBRIR_INC, VBRIR_CS and nVBRIR_UnD. The control signals are based on DALLAS DS1804 NV Trimmer Potentiometer to design. Users could check the "*Advantech SOM-A255x series CSB design guide* "to know how to wire. User could check appendix about SOM-A255F memory map to know how to control.

If user wants to connect CSB to LVDS type LCD, user could reference "*Advantech SOM-A255x series CSB design guide* "to design LVDS Transmitter on CSB. SOM-A255x series only support 1 channel LVDS LCD panel.

The sample images of SOM-A2552, SOM-A255F series could support 4 kinds of display modes:

- **320x240 TFT**: In SOM-A2552 & SOM-A255F module, user CAN'T verify the performance by Advantech LCD kit LCD-A057-STQ1-0. Because SOM-A2552 & SOM-A255F supports 320x240 TFT mode, but LCD-A057-STQ1-0 is 320x240 STN panel.
- **640x480 TFT**: user could verify the performance by Advantech LCD kit LCD-A064-TTV1-0.
- **800x600 TFT**: user could verify the performance by Advantech LCD kit LCD-A104-TTS1-0.
- **1024x768 TFT**: user could verify the performance by Advantech LCD kit LCD-A150-TTX2-0.

Except 320x240 TFT mode, user could verify the LCD-out function by Advantech LCD kit. Advantech LCD kit LCD-A057-STQ1-0 is 320x240 STN type LCD, not TFT type, so user couldn't verify the 320x240 TFT function by sample images.

The sample images of SOM-A2558 series could support 4 kinds of display modes:

- **320x240 STN**: User can use Advantech LCD kit LCD-A057-STQ1-0 to evaluate the LCD-out performance of SOM-A2558 platform.
- **640x480 TFT**: User can use Advantech LCD kit LCD-A064-TTV1-0 to evaluate the LCD-out performance of SOM-A2558 platform.

2.2.11 Zoom Video (ZV) port

SOM-A255F & SOM-A2552 series ZV port comes from SM501. SOM-A2558 series don't support the function. ZV Port can interface with video decoders, such as NTSC/PAL decoders, MPEG-2 decoders, and JPEG Codec. The ZV Port supports resolutions up to 1280x1024. It directly accepts digitized RGB or YUV signals, and does not accept analog signals.

In 16-bit mode, the ZV [15:8] signals are the most-significant eight video pixel inputs. In 8-bit mode, these signals are not used. In 16-bit mode, the ZV [7:0] signals are the least-significant eight video pixel inputs. In 8-bit mode, these signals are the only eight video pixel inputs.

About how to wire the ZV port with NTSC/PAL decoders, please check "*Advantech SOM-A255x series CSB design guide* ".

2.2.12 System Reset Interface

SOM-A255x series all supply 3 kinds of System reset interface as following:

➢ nRESET : hardware reset input pin. The pin is pulled high in SOM-A255F. The pin is triggered by signal falling edge.

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> ➢ nSW_RESET : software rest input pin. The pin is pulled high in SOM-A255F. The pin is triggered by signal falling edge.
> ➢ nSA_PWR_ON : Suspend/wake-up pin. The pin is pulled high in SOM-A255F. The pin is triggered by signal falling edge.

2.2.13 Buzzer Control Interface

SOM-A255x series all support this function. Buzzer-out control signal is designed to control the buzzer on/off status.

If users want to design buzzer on CSB to be reminding or alarm system, user could reference "*Advantech SOM-A255x series CSB design guide* ".

If users want to control the buzzer, users can check the memory map to do it.

2.2.14 System Management Bus (SM Bus) interface

SOM-A255x series SM Bus is implemented by PXA255 I2C bus. If users' CSB is powered by battery pack with SM bus battery gauge IC, then users could connect the SOM-A255x SM Bus to battery pack to monitor battery status. SOM-A255x series SM bus directly support TI BQ2040 gas gauge IC.

2.2.15 Power-input

SOM-A255x needs 3.3V & 5V DC power inputs. The power sources (3.3V, 5V) must always be supplied even in system sleep mode. SOM-A255x power management is completely implemented on itself; users' CSB doesn't need to control the power supply to SOM-A255x.

2.2.16 Back-up power input

If user want to keep the real time clock(RTC) works well in power off mode, user should connect the coin battery positive pin to BAT-VCC in X2 directly .The back-up power pin (BAT_VCC) is the only power source to supply RTC power when SOM-A255x system power (3.3V, 5V) is off.

The coin battery must be 3.0V Li-ion coin type.

The coin battery charging circuit is designed on SOM-A255x, so user shouldn't and needn't design the charging circuit on CSB.

If users don't need RTC function in CSB, just let the BAT_VCC pin open.

2.2.17 PCI I/F (Thru X3)

SOM-A2558 & SOM-A255F could support 4 channels PCI device controllers on CSB. The PCI clock is 33 MHz. PCI I/F comes from Advantech EVA-C210 I/O enhancement chip. The PCI I/F feature is as followings:

- Compatible with PCI specification version 2.2

- 32-bit data bus interface

- Built-in PCI bus arbiter

- Supports up to 3 individual external bus master devices

- Support PCI Bus Controller (FPCI) to PCI slave I/O read/write,

  memory read/write, configuration read/write cycle

- PCI Bus master support all disconnect types (Master-Abort,

  Target-Abort, Target-Retry, Disconnect with data, Disconnect without

data)

SOM-A2552 series don't support PCI I/F.

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