

Dell PowerEdge C5230
Systems

Hardware Owner's Manual

Regulatory Model: B04S



Notes, Cautions, and Warnings



NOTE: A NOTE indicates important information that helps you make better use of your system.



CAUTION: A CAUTION indicates potential damage to hardware or loss of data if instructions are not followed.



WARNING: A WARNING indicates a potential for property damage, personal injury, or death.

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Regulatory Model: B04S

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Important Information

- Your system must have BIOS version 1.0.2 or later to support Intel Xeon E3-1200 v3 series processors. You can download the latest version of the BIOS at dell.com/support.
- Your system must have the BMC version 1.00 or later to support Intel Xeon E3-1200 v3 series processors. You can download the latest version of the BMC firmware at dell.com/support.
- Your system must have the Backplane firmware version 1.12 or later to support Intel Xeon E3-1200 v3 series processors. You can download the latest version of the Backplane firmware at dell.com/support.


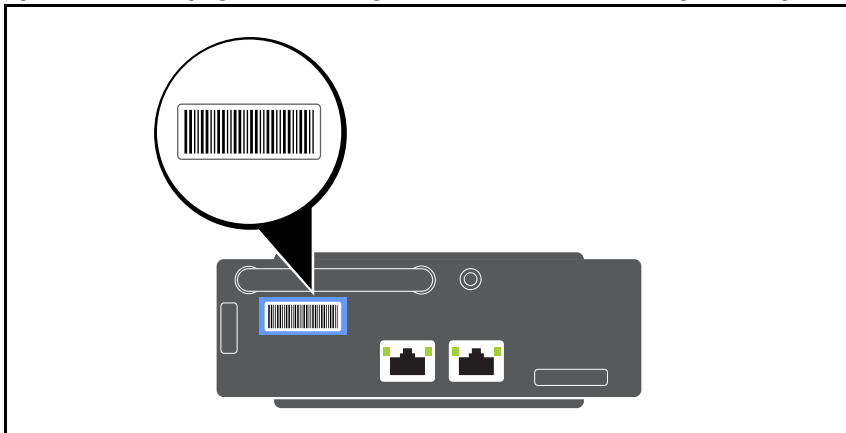
 **NOTE:** PowerEdge C5230 systems with a service tag on the front panel support only Intel Xeon E3-1200 series.

Figure 1-1. Identifying the Service Tag on the Front Panel of PowerEdge C5230 Systems.



About Your System

The system includes the following configurations:

- 12-sled system supporting 3.5 inch hard drives.
- 12-sled system supporting 2.5 inch hard drives.



NOTE: Supporting SATA drive only, SAS driver is not supported.

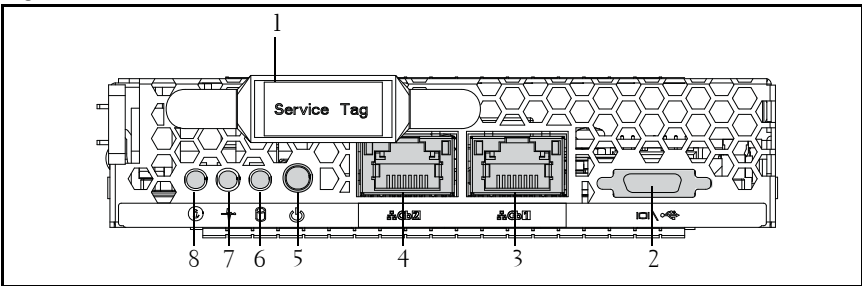
Front-Panel Features and Indicators

The Dell PowerEdge C5230 server is available in a 12-sled system supporting either two 3.5-inch or four 2.5-inch hard drives. For information on sled population, see "Sled Configuration" on page 101.

The following section provides information for the 12-sled and mezzanine card options.

Features

Figure 1-2. 12-Sled SKU Front Panel Features (Rotated Counterclockwise 90°)



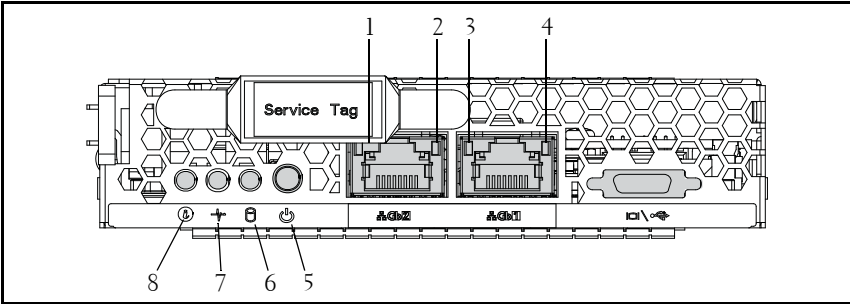
Item	Feature	Description
1	Service Tag	Identifying service tag
2	Y-cable connector	USB (x2) + VGA
3	NIC1 LAN port	10/100/1G NIC LAN
4	NIC2 LAN port	
5	Power button	On/Off button for sled
6	HDD LED	Active LED for HDD
7	Status LED	Indicates the state of varying system events.
8	ID LED	Indicator for system identifier



NOTE: PowerEdge C5230 systems with a service tag on the front panel support Intel Xeon E3-1200 series processors only.

Indicators

Figure 1-3. Front Panel Indicators (Rotated Counterclockwise 90°)



Item	Feature	Status	Description
2, 4	LAN link LED	Off	No link
1, 3	LAN activity LED	Off	No activity
	LAN link LED	Green	Link
	LAN activity LED	Off	No activity
	LAN link LED	Green	Link
	LAN activity LED	Off	Activity 10 Mb
	LAN link LED	Blinking green	Link
	LAN activity LED	Green	Activity 100 Mb
	LAN link LED	Blinking green	Link
	LAN activity LED	Amber	Activity 1Gb
5	Power LED	Green	System DC On
		On	
		Off	System DC Off

6	Hard drive activity LEDs	Blinking green	Hard drive 0 active Hard drive 1 active Hard drive 2 active Hard drive 3 active
7	Status LED	Amber Off	Normal status
		Blinking amber	Event occurred in the system
8	Identity LED	Blue On Blue Off Blinking blue	Identifies the system Normal status Identifies the system with an interval

Using the System Setup Program

Start Menu

The system employs the latest AMI Core BIOS, which is stored in Flash memory. The Flash memory supports the plug-and-play specification, and contains a BIOS Setup program, the Power On Self Test (POST) routine, and the PCI auto-configuration utility.

This system board supports system BIOS shadowing enabling the BIOS to execute from 64-bit onboard write-protected DRAM.

Use the Setup Utility to configure items such as:

- Hard drives and peripherals
- Memory sizing and configuration
- Password protection from unauthorized use
- Protocol and feature enabling/disabling
- Power Management features

This Setup utility should be executed under the following conditions:

- When changing the system configuration
- When a configuration error is detected by the system and you are prompted to make changes to the Setup utility
- When redefining the communication ports to prevent any conflicts
- When changing the password or making other changes to the security setup



NOTE: Only items in brackets [] can be modified. Items that are not in brackets are display only.

BIOS Setup Options at Boot

The user initiates SETUP by pressing <F2> during POST.

Console Redirection

The console redirection allows a remote user to diagnose and fix problems on a server, which has not successfully booted to the operating system. The centerpiece of the console redirection is the BIOS Console. The BIOS Console is a Flash ROM-resident utility that redirects input and output over a serial or modem connection.

BIOS supports redirection of both video and keyboard through a serial link (serial port). After enabling console redirection, the local (host server) keyboard input and video output are accessible by the local keyboard and video connections.

Operation through the remote console without the need for a local keyboard or monitor is also available.



NOTE: Full compatibility and functionality for the available emulation standards may vary.

Enable/Disable Console Redirection

The console redirection function can be enabled/disabled in the BIOS Setup menu. See "Remote Access Configuration" on page 54.

Configuring Special Keys

Console redirection uses ANSI terminal emulation, which is limited to basic ASCII characters. There are no function keys, arrow keys, or control keys in this character set. However, the PowerEdge C5230 software requires the use of function keys and control keys for ordinary functions. You can emulate a function key or control key by using a special key sequence called an escape sequence, to represent a specific key.

For console redirection, an escape sequence starts with an escape character. This character can be entered in a variety of different ways depending on the requirements of your terminal emulation software. For example, 0x1b, ^[, and <Esc> refer to the same escape character.

The following table lists the escape sequence that must be sent to represent a special key or command.

Key	ANSI Escape Sequence	Other Sequences
F1	<ESC><Shift>op	<ESC>1
F2	<ESC><Shift>oq	<ESC>2
F3	<ESC><Shift>or	<ESC>3
F4	<ESC><Shift>os	<ESC>4
F5		<ESC>5
F6		<ESC>6
F7		<ESC>7
F8		<ESC>8
F9		<ESC>9
F10		<ESC>0
F11		<ESC>!
F12		<ESC>@
Home	<ESC>[<Shift>h	<ESC>h
End	<ESC>[<Shift>k	<ESC>k
Ins		<ESC>+
Del		<ESC>-
Page Up		<ESC>?

Key	ANSI Escape Sequence	Other Sequences
Page Down		<ESC>/
Reset		<ESC>R<ESC>r <ESC>R

General Help

In addition to the Item Specific Help window, the Setup Utility also provides a General Help screen. This screen can be called up from any menu by pressing <F1>. The General Help screen lists the legend keys with their corresponding alternates and functions. To exit the help window, press the <Enter> or the <Esc> key.

Server Platform Setup Utility Screens

Conventions

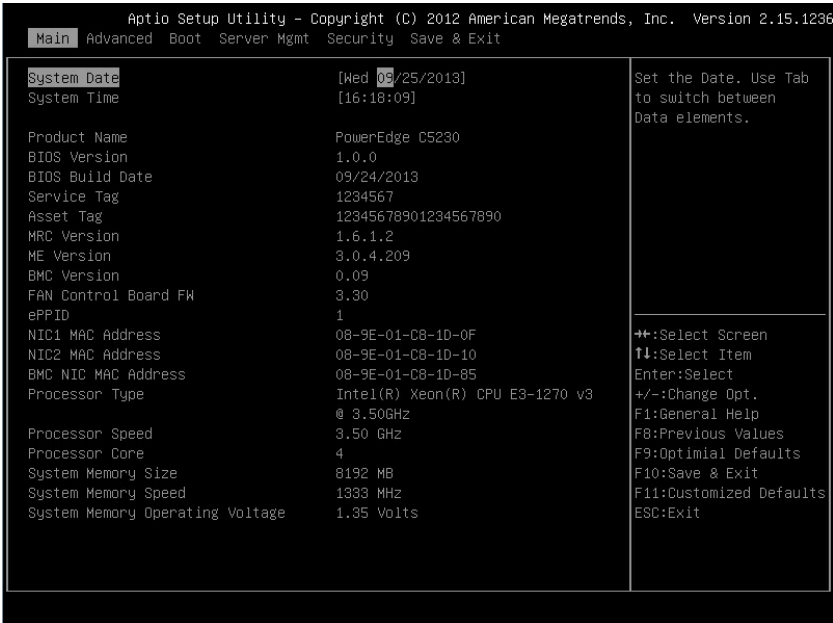
The following typographical conventions are used in the tables:

- The text and values in the Setup Item, Options, and Help columns in the tables are displayed on the BIOS Setup screens.
- Text marked with an * in the Settings column of the tables indicates default values. These values are not displayed with an * on the setup screen. The marked text in this document is to serve as a reference point.
- The Comments column provides additional information where it may be helpful. This information does not appear in the BIOS Setup screens.
- Information in the screen shots that is enclosed in brackets (< >) indicates variables, depending on the option(s) installed. For example <Current Date> is replaced by the actual current date.
- Information that is enclosed in square brackets ([]) in the tables indicates areas where the user needs to type in text instead of selecting from a provided option.
- Whenever information is changed (except Date and Time) the systems requires a save and reboot to take place. Pressing <ESC> discards the changes and boot the system according to the boot order set from the last boot.

Main Menu

The Main menu is the screen that is first displayed when you enter BIOS Setup.

Figure 2-1. Main Menu Screen



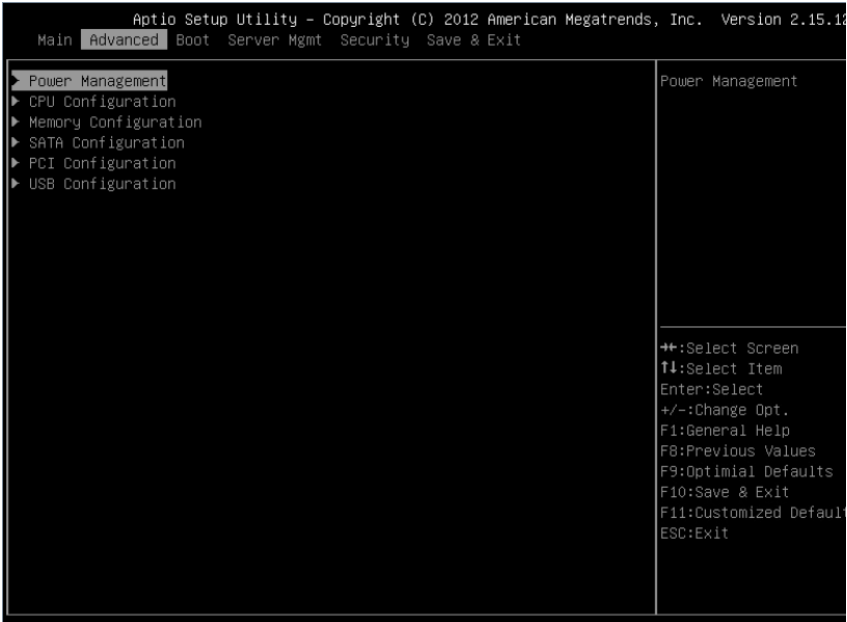
Menu Fields	Settings	Comments
Main		
System Date	MM/DD/YYYY	Set the Date. Use <Tab> to switch between Date elements.
System Time	HH:MM:SS	Set the time. Use <Tab> to switch between Time elements.
Product Name		Displays the product name.
BIOS Version		Displays the BIOS version.

Menu Fields	Settings	Comments
BIOS Build Date		Displays the BIOS build date.
Service Tag		Displays the service tag.
Asset Tag		Displays the asset tag.
MRC Version		Displays the MRC version.
ME Version		Displays the ME version.
BMC Version		Displays the BMC version.
FAN Control Board FW		Displays the fan control board firmware version.
ePPID		Displays the ePPID.
NIC1 MAC Address		Displays the NIC1 MAC address.
NIC2 MAC Address		Displays the NIC2 MAC address.
BMC NIC MAC Address		Displays the BMC NIC MAC address.
Processor Type		Displays the processor type.
Processor Speed		Displays the processor speed.
Processor Core		Displays the amount of processor core.
System Memory Size		Displays the amount of system memory.
System Memory Speed		Displays the memory speed.
System Memory Operating Voltage		Displays the system memory operating voltage.

Advanced Menu

The Advanced screen provides an access point to configure several options. On this screen, the user selects the option that is to be configured. Configurations are performed on the selected screen, not directly on the Advanced screen.

Figure 2-2. Advanced Menu Screen



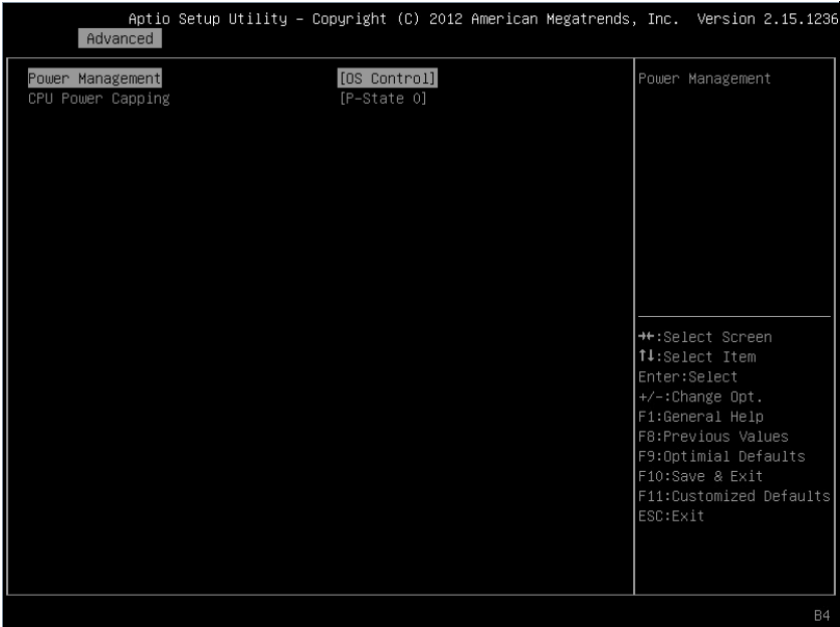
⚠ CAUTION: Incorrect settings to items on the Advanced Menus may cause the system to malfunction. Unless you have experience adjusting these items, we recommend that you do not adjust the default values. If the system malfunctions or does not boot after changing the settings, open BIOS and choose "Load Optimal Defaults" in the Exit menu to boot up normally.

Menu Fields	Settings	Comments
Advanced		
Power Management		Power Management.

Menu Fields	Settings	Comments
CPU Configuration		CPU Configuration.
Memory Configuration		Memory Configuration.
SATA Configuration		SATA Devices Configuration.
PCI Configuration		PCI, PCI-X and PCI Express Settings.
USB Configuration		USB Configuration.

Power Management

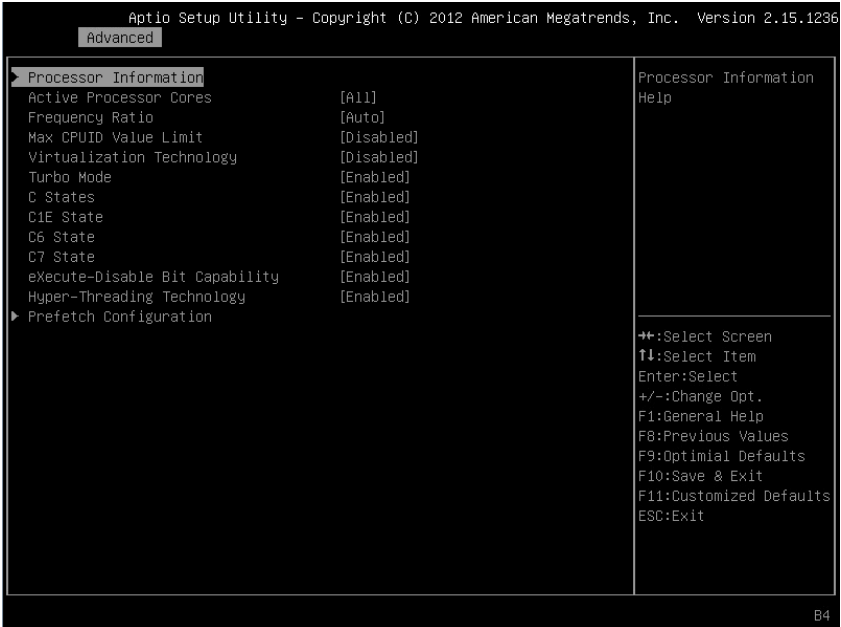
Figure 2-3. Power Management Screen



Menu Fields	Settings	Comments
Advanced \Power Management		
Power management	Maximum Performance OS Control*	Power management.
CPU power capping	P-state 0* P-state 1 P-state 2 P-state 3 P-state 4	CPU power capping.

CPU Configuration

Figure 2-4. CPU Configuration Screen



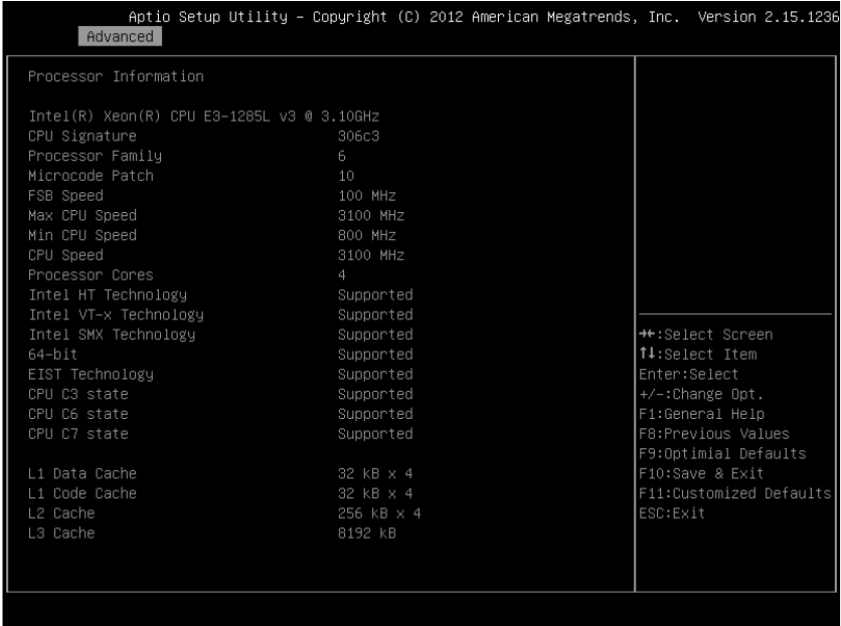
Menu Fields	Settings	Comments
Advanced\CPU Configuration		
Processor Information		
Active Processor Cores	All*	Number of cores to enable in each processor package.
	1	
	2	
	4	
Frequency Ratio	Auto	The Level of CPU Frequency.
	1	
	2	
	3	

Menu Fields	Settings	Comments
Max CPUID Value Limit	Disabled* Enabled	Some OS's (NT4) will fail if the value returned in EAX is > 3 when CPUID instruction is executed with EAX=0. This setting limits CPUID function to 3 or disable it.
Virtualization Technology	Disabled* Enabled	This feature will allow the users to disable/enable the VT technology in applicable CPUs. If disabled, the VT feature is unusable in any OS.
Turbo Mode	Disabled Enabled*	Turbo Mode.
C States	Disabled Enabled*	Set to disable, there are no C states available for the processor. Set to enable (default), the processor can operate in all available Power C States.
C1E State	Disabled Enabled*	Set C1E disabled/enabled.
C6 State	Disabled Enabled*	Set C6 disabled/enabled.
C7 State	Disabled Enabled*	Set C7 disabled/enabled.

Menu Fields	Settings	Comments
eXecute-Disable Bit Capability	Disabled Enabled*	When disable, Intel CPUs that support the eXecute Disable (XD) feature will not report the support to the operating system. When enable, Intel CPUs that support the eXecute Disable (XD) feature will report the support to the operating system.
Hyper-Threading Technology	Disabled Enabled*	Disable/Enable Hyper-Threading Technology.
Prefetch Configuration		Prefetch Configuration

Processor Information

Figure 2-5. Processor Information Screen



Prefetch Configuration

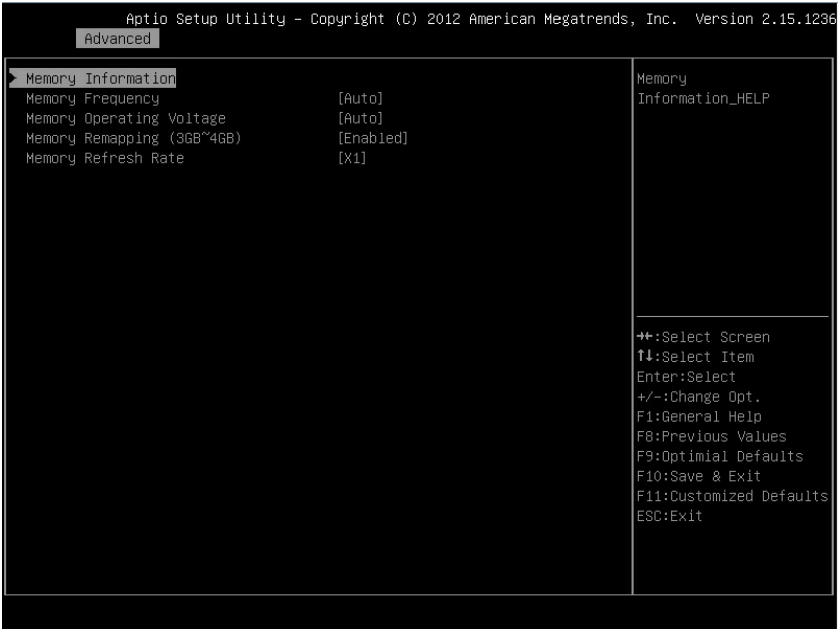
Figure 2-6. Prefetch Configuration Screen



Menu Fields	Settings	Comments
Advanced\CPU Configuration\Prefetch Configuration		
Adjacent Cache Line Prefetch	Disable Enable*	To turn on/off prefetching of adjacent cache lines.
Hardware Prefetcher	Disable Enable*	To turn on/off the Mid Level Cache (L2) streamer prefetcher.

Memory Configuration

Figure 2-7. Memory Configuration Screen

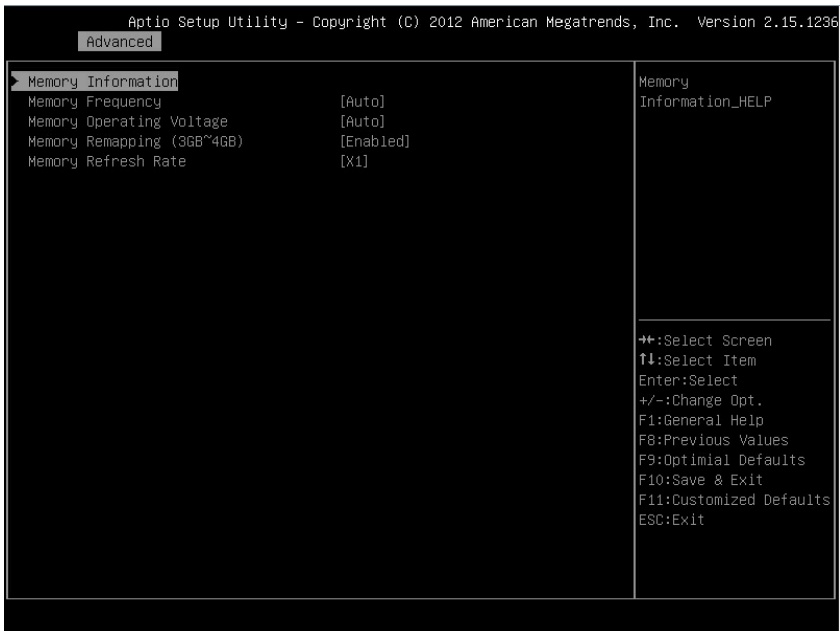


Menu Fields	Settings	Comments
Advanced\Memory Configuration		
Memory Frequency	Auto* 1066 MHz 1333 MHz 1600 MHz	Auto-Detect the memory running speed or set running speed up to 1066/1333/1600 MHz.

Menu Fields	Settings	Comments
Memory Operating Voltage	Auto* 1.5V 1.35V	Memory operating voltage will be set automatically by the Memory initialization code and depends upon the installed DIMM's capability and the memory configuration of the system or set it 1.5/1.35 volts.
Memory Remapping (3 GB - 4 GB)	Enabled* Disabled	Memory remapping relocates memory space 3 GB~4 GB to the space above 4 GB with this feature disabled/enabled.

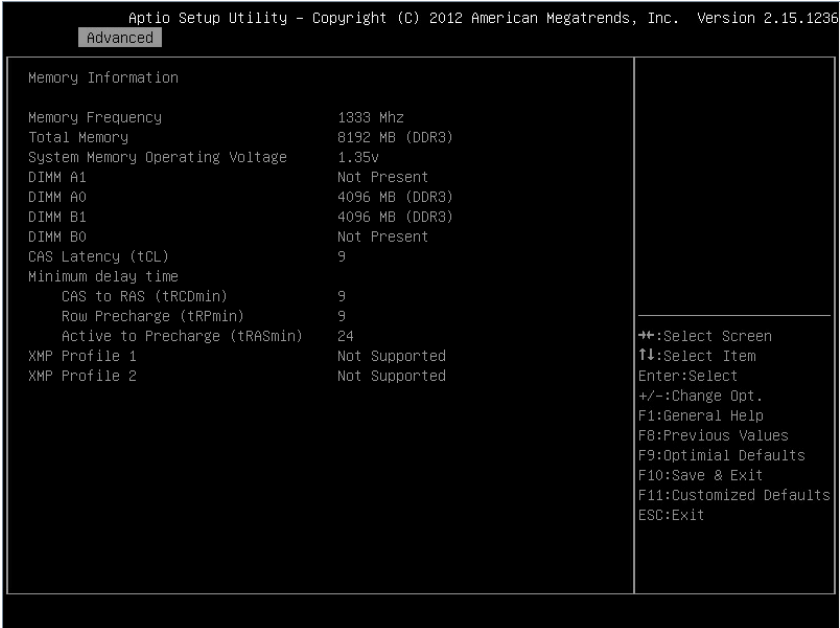
Memory Configuration

Figure 2-8. Memory Configuration Screen



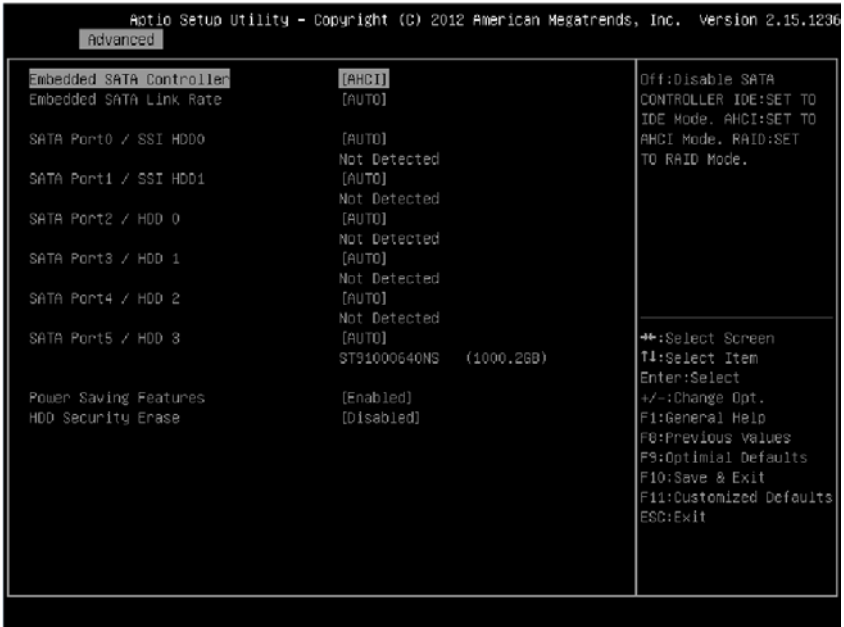
Memory Information

Figure 2-9. Memory Information Screen



SATA Configuration

Figure 2-10. SATA Configuration Screen



Menu Fields	Settings	Comments
Advanced\SATA Configuration		
Embedded SATA Controller	Off	Disables the SATA controller or enables it and sets the device class code as IDE/AHCI/RAID. This token applies to the first on-board SATA controller.
	IDE	
	AHCI*	
	RAID	
Embedded SATA Link Rate	Auto*	Forces the SATA port to run at GEN1 mode if this option is set to 1.5 Gbps. Setting to Auto will leave the port to run at default mode.
	1.5 Gbps	
	3.0 Gbps	

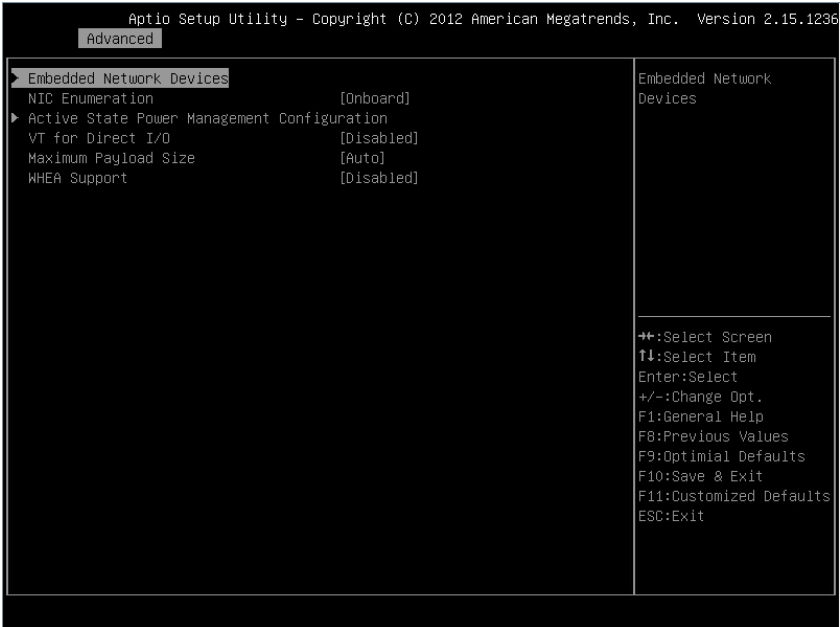
Menu Fields	Settings	Comments
SATA Port0 / SSI HDD0	OFF Auto*	While entering setup, BIOS auto detects the presence of SATA devices and displays the status of detected SATA hard drives.
SATA Port1 / SSI HDD1	OFF Auto*	While entering setup, BIOS auto detects the presence of SATA devices and displays the status of detected SATA hard drives.
SATA Port2 / HDD0	OFF Auto*	While entering setup, BIOS auto detects the presence of SATA devices and displays the status of detected SATA hard drives.
SATA Port3 / HDD1	OFF Auto*	While entering setup, BIOS auto detects the presence of SATA devices and displays the status of detected SATA hard drives.
SATA Port4 / HDD2	OFF Auto*	While entering setup, BIOS auto detects the presence of SATA devices and displays the status of detected SATA hard drives.
SATA Port5 / HDD3	OFF Auto*	While entering setup, BIOS auto detects the presence of SATA devices and displays the status of detected SATA hard drives.
Power Saving Features	Disabled Enabled*	Disable/Enable the feature that allows SATA hard drives to initiate link power management transitions.
HDD Security Erase	Disabled* Enabled	Not Set Security Freeze Lock Command.

Port Mapping of Cougar Point SATA Controllers

SATA Port0 / SSI HDD0	Bus0:Dev31:Fun2 SATA Controller
SATA Port1 / SSI HDD1	Bus0:Dev31:Fun2 SATA Controller
SATA Port2 / HDD0	Bus0:Dev31:Fun2 SATA Controller
SATA Port3 / HDD1	Bus0:Dev31:Fun2 SATA Controller
SATA Port4 / HDD2	Bus0:Dev31:Fun5 SATA Controller
SATA Port5 / HDD3	Bus0:Dev31:Fun5 SATA Controller

PCI Configuration

Figure 2-11. PCI Configuration Screen



Menu Fields	Settings	Comments
Advanced\PCI Configuration		
Embedded Network Devices		Embedded Network Devices.
NIC Enumeration	Onboard* Add-in	Change the sequence of NIC OPROM initialization.
Active State Power Management Configuration		Active State Power Management Configuration.

Menu Fields	Settings	Comments
VT for Direct I/O	Disable* Enable	Disable/Enable Intel Virtualization Technology for Direct I/O (VT-d) that enhances I/O support (DMA) when running a Virtual Machine Monitor.
Maximum Payload Size	Auto* 128 Bytes 256 Bytes	Auto detects the PCIe maximum payload size or sets it to 128/256 Bytes.
WHEA Support	Disable* Enable	Enable or disable Windows Hardware Error Architecture (WHEA).

Embedded Network Devices

Figure 2-12. Embedded Network Devices Screen

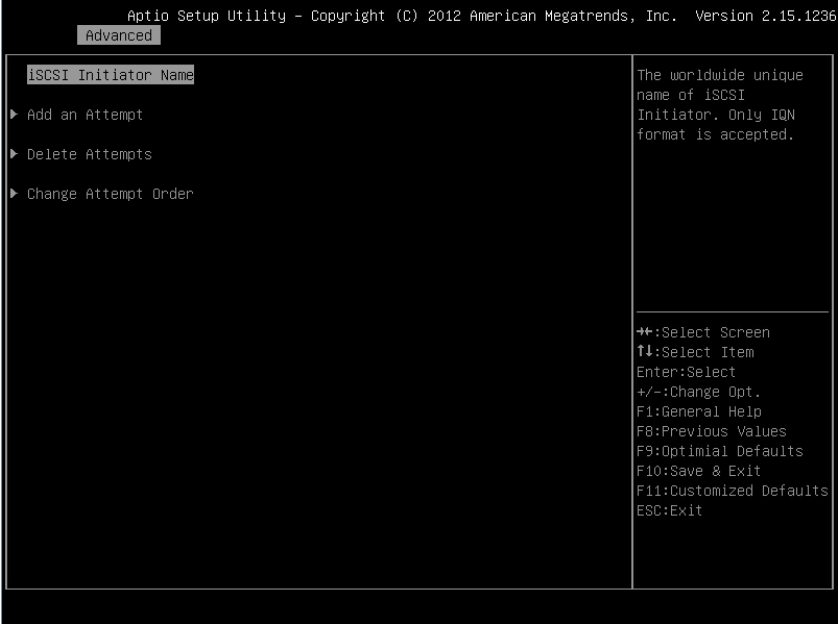


Menu Fields	Settings	Comments
Advanced\PCI Configuration\Embedded Network Devices		
Embedded NIC1	Disabled Enabled with PXE* Enabled without PXE iSCSI Remote Boot	Disable/Enable the system's primary embedded network interface controller (full-function), w/, w/o including its PXE boot-ROM or with iSCSI Remote Boot. To disable NIC1, NIC2 should be disabled first. If iSCSI is enabled, UEFI PXE can not boot.

Menu Fields	Settings	Comments
Embedded NIC2	Disabled Enabled with PXE Enabled without PXE* iSCSI Remote Boot	Disables/Enables the system's secondary embedded network interface controller (full-function), w/, w/o including its PXE boot-ROM or with iSCSI Remote Boot. If iSCSI is enabled, UEFI PXE can not boot.
iSCSI Configuration		Configure the iSCSI parameters. This page appears and allows to setup while boot mode is set to UEFI mode and one of NIC1 and NIC2 is set to iSCSI Remote Boot.

iSCSI Configuration

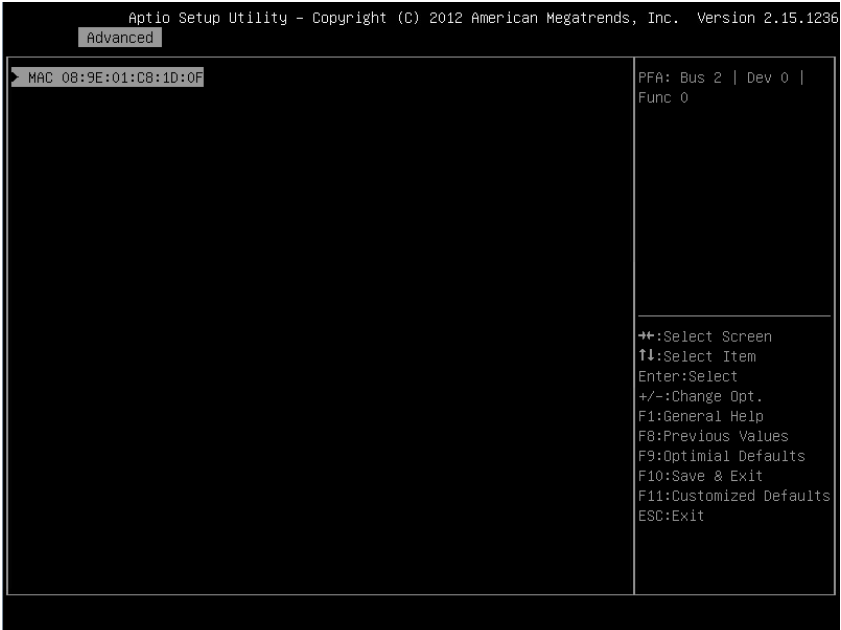
Figure 2-13. iSCSI Configuration Screen



Menu Fields	Settings	Comments
Advanced\PCI Configuration\Embedded Network Devices\iSCSI Configuration		
iSCSI Initiator Name		The worldwide unique name of iSCSI Initiator. Only IQN format is accepted.
Add an attempt		Add an Attempt.

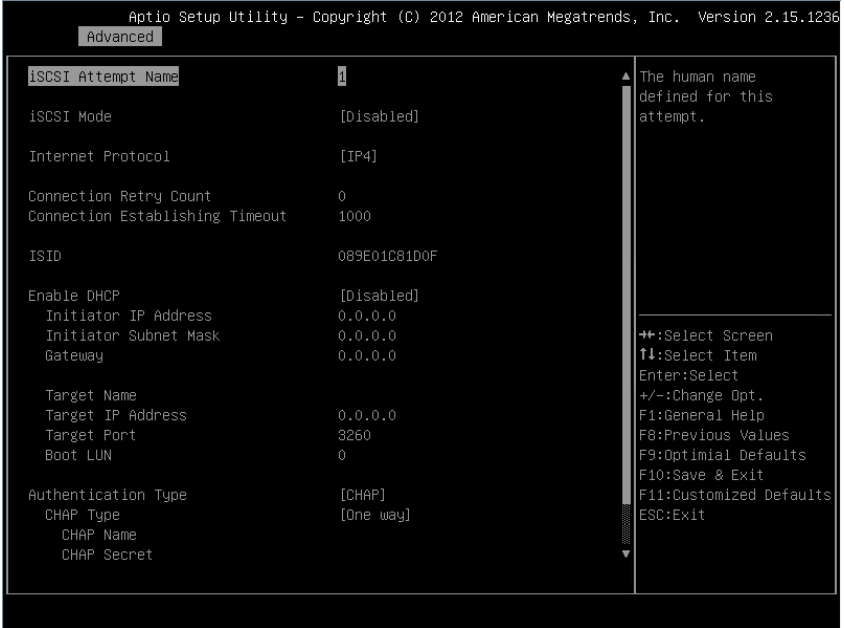
Menu Fields	Settings	Comments
Delete Attempts		Delete one or more attempts.
Change attempt order		Change the order of Attempts using +/- keys. Use arrow keys to select the attempt then press +/- to move the attempt up/down in the attempt order list.

Figure 2-14. iSCSI Configuration Advanced Screen



Menu Fields	Settings	Comments
Advanced\PCI Configuration\Embedded Network Devices\iSCSI Configuration\Add an Attempt		
MAC xx:xx:xx:xx:xx:xx		PFA: BUSx Devx Func x. MAC address and BUS/Dev/Fun are dependent on platform.

Figure 2-15. iSCSI Attempt Name Screen



Menu Fields	Settings	Comments
Advanced\PCI Configuration\Embedded Network Devices\iSCSI Configuration\Add an Attempt		
iSCSI Attempt Name		The human name defined for this attempt.
iSCSI Mode	Disabled* Enabled Enabled for MPIO	Disabled, Enabled, Enabled for MPIO.

Menu Fields	Settings	Comments
Internet Protocol	IP4* IP6 Autoconfigure	Initiator IP address is system assigned in IP6 mode. In Autoconfigure mode, iSCSI driver will attempt to connect iSCSI target via IPv4 stack, if failed then attempt IPv6 stack.
Connect Retry Count		The minimum value is 0 and the maximum is 16. 0 means no retry.
Connection Establishing Time out		The timeout value in milliseconds. The minimum value is 100 milliseconds and the maximum is 20 seconds.
ISID		Information only. Display MAC Address.
Enable DHCP	Disabled* Enabled	Enable DHCP
Initiator IP address		Enter IP address in dotted-decimal notation.
Initiator Subnet Mask		Enter IP address in dotted-decimal notation.
Gateway		Enter IP address in dotted-decimal notation.
Target Name		The worldwide unique name of iSCSI Initiator. Only IQN format is accepted.
Target IP address		Enter IP address in dotted-decimal notation.
Target Port		Target Port

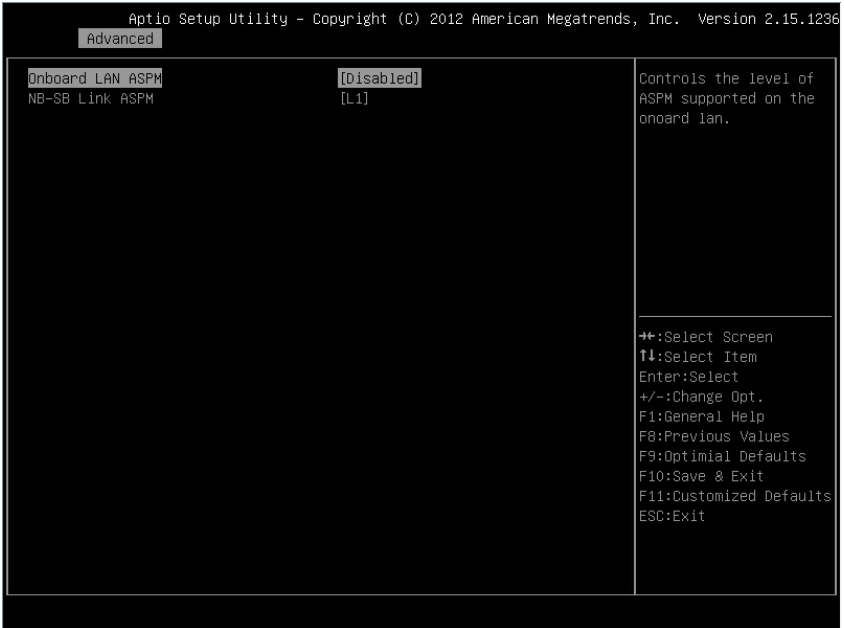
Menu Fields	Settings	Comments
Boot LUN		Hexadecimal representation of the LU number. Examples are : 4752-3A4F-6b7e-2F99, 6734-9-156f-127, 4186-9
Authentication Type	CHAP* None	Authentication method: CHAP, Kerberos, or None.
CHAP Type	One way* Mutual	None, One way CHAP or Mutual CHAP.
CHAP Name		CHAP Name
CHAP Secret		The minimum length is 12 bytes and the maximum length is 16 bytes.
Save Changes		Must reboot system manually for changes to take place.
Back to Previous Page		Back to Previous Page.

Figure 2-16. iSCSI Configuration Delete an Attempt Screen



Menu Fields	Settings	Comments
Advanced\PCI Configuration\Embedded Network Devices\iSCSI Configuration\Delete Attempt		
Commit Changes and Exit		Commit Changes and Exit.
Discard Changes and Exit		Discard Changes and Exit.

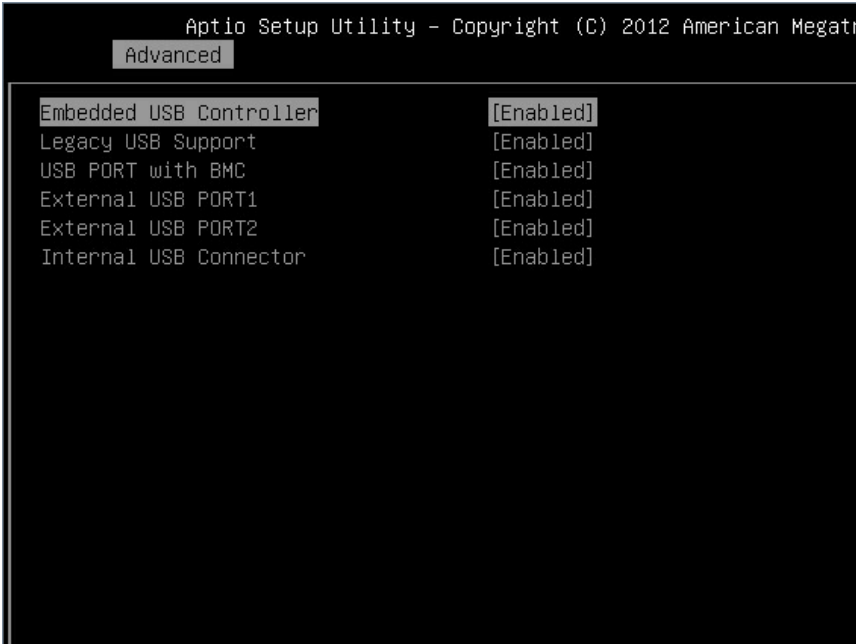
Figure 2-17. iSCSI Active State Power Management Configuration Screen



Menu Fields	Settings	Comments
Advanced\PCI Configuration\Active State Power Management Configuration		
Onboard LAN ASPM	Disabled* L0s L1 L0s & L1	Controls the level of ASPM supported on the PCI Express Link.
NB-SB Link ASPM	Disabled L1*	Controls the level of ASPM supported on the PCI Express Link.

USB Configuration

Figure 2-18. USB Configuration Screen



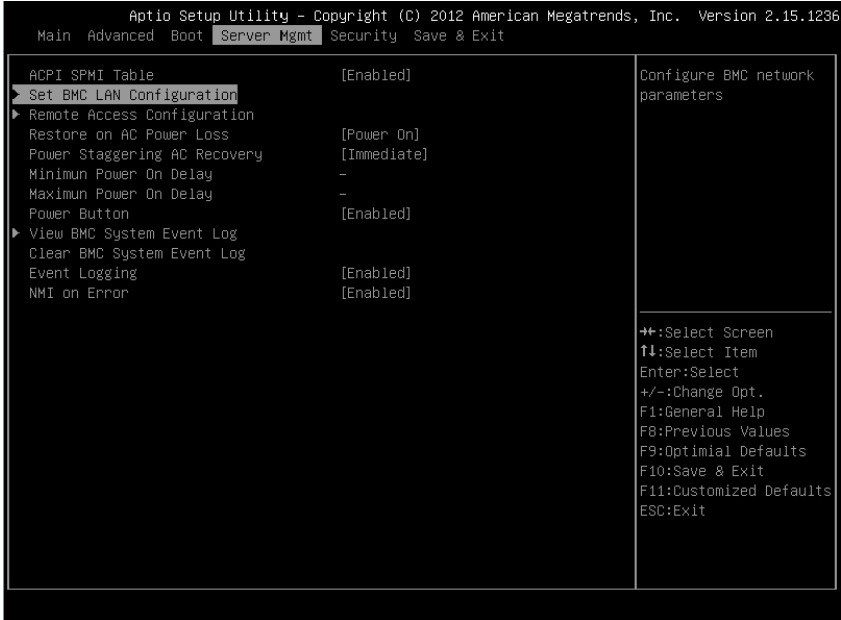
Menu Fields	Settings	Comments
Advanced\USB Configuration		
Embedded USB Controller	Disabled	Disables/Enables the built-in USB controller at system startup.
	Enabled*	
Legacy USB Support	Disabled	Enables Legacy USB support. Disable option keeps USB devices available only for EFI applications.
	Enabled*	

Menu Fields	Settings	Comments
USB PORT with BMC	Disabled Enabled*	Allows the users to electrically disable/enable the internal USB port which contacts to BMC.
External USB PORT1	Disabled Enabled*	Allows the users to electrically disable/enable the external USB port1.
External USB PORT2	Disabled Enabled*	Allows the users to electrically disable/enable the external USB port2.
Internal USB Connector	Disabled Enabled*	Disables/Enables the internal USB port.

Boot Menu

This page enables you to set POST boot parameters.

Figure 2-19. Boot Menu Screen



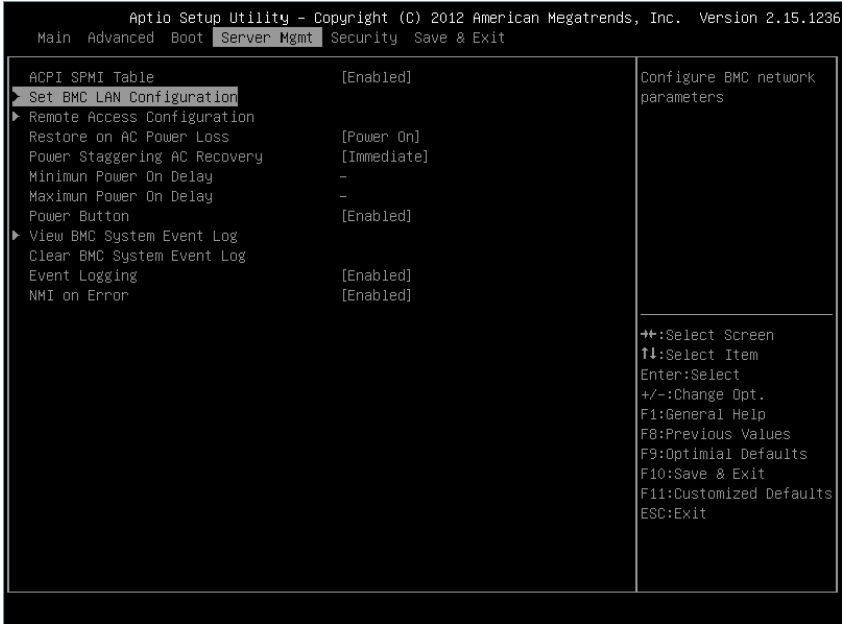
Menu Fields	Settings	Comments
Boot		
Quiet Boot	Disabled Enabled*	Enables or disables Quiet Boot option.
Pause On Errors	Disabled* Enabled	Pause on Errors.
Force PXE Boot Only	Disabled* Enabled	Force PXE Boot Only.

Menu Fields	Settings	Comments
Boot Mode	BIOS* UEFI	If Boot Mode UEFI/BIOS is selected, only UEFI legacy boot devices are selected for bootup.
MenuPXE Boot Protocol	IPv4* IPv6	Appear and allow to select while boot mode set to UEFI mode.
1st Boot	Network* Hard Disk RAID USB Storage CD/DVD	Set Boot Priority
2nd Boot	Network Hard Disk* RAID USB Storage CD/DVD	Set Boot Priority
3rd Boot	Network Hard Disk RAID* USB Storage CD/DVD	Set Boot Priority
4th Boot	Network Hard Disk RAID USB Storage* CD/DVD	Set Boot Priority

Menu Fields	Settings	Comments
5th Boot	Network Hard Disk RAID USB Storage CD/DVD*	Set Boot Priority

Server Management

Figure 2-20. Server Management Screen

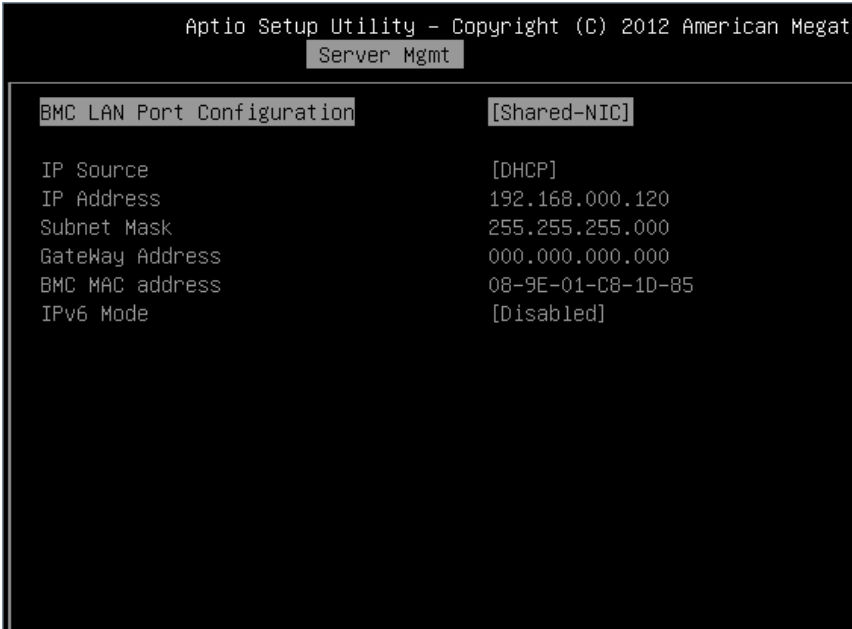


Menu Fields	Settings	Comments
Server Management		
ACPI SPMI Table	Disabled Enabled*	ACPI SPMI Table.
Set BMC LAN Configuration		Configures BMC network parameters.
Remote Access Configuration		Remote Access Configuration.
Restore on AC Power Loss	Power Off Power On* Last State	System action to take on AC power loss.

Menu Fields	Settings	Comments
Power Staggering AC Recovery	Immediate* Random User Defined	Immediate: PowerOn (No Delay)\Random: (Auto)\User Defined: user defined delay time must be in the range of Minimum and Maximum Power On Delay.
Power Button	Disabled Enabled*	Select Disabled to disable power off function.
View System Event Log		Press <Enter> to view system Event Log records.
Clear BMC System Event Log		Choose options for erasing SEL.
Event logging	Disabled Enabled*	Disable PCIE SERR/DRAM ECC Error Logging.
NMI On Error	Disabled Enabled*	Enable or disable NMI asserted for fatal error.

Set BMC LAN Configuration

Figure 2-21. Set BMC LAN Configuration Screen

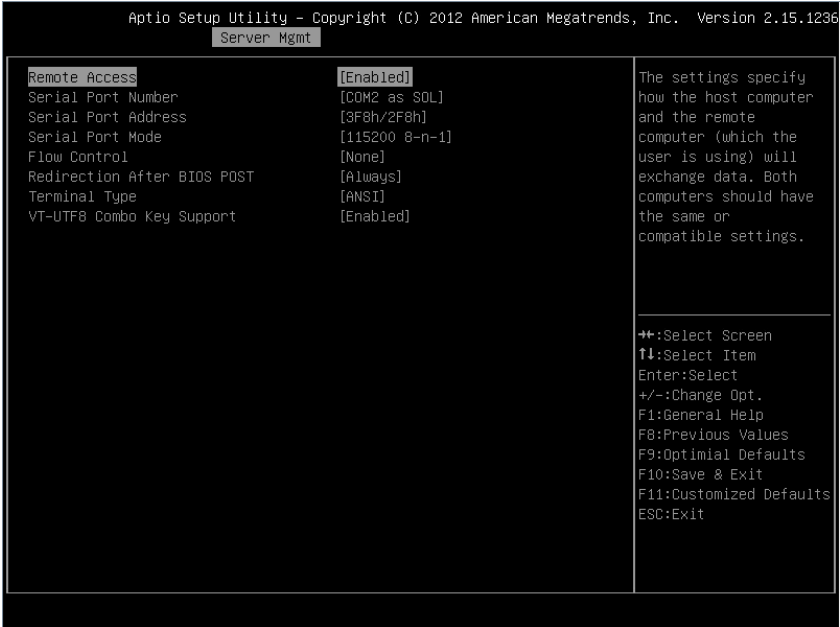


Menu Fields	Settings	Comments
Server Management/BMC Network Configuration		
BMC LAN Port Configuration	Dedicated-NIC Shared-NIC*	BMC LAN Port Configuration.
BMC NIC IP Source	Static DHCP*	Select to configure LAN channel parameters statically or dynamically (DHCP). Do nothing option will not modify any BMC network parameters during BIOS phase.

Menu Fields	Settings	Comments
IP Address	xxx.xxx.xxx.xxx	Enter IP address in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only).
Subnet Mask	xxx.xxx.xxx.xxx	Enter Subnet Mask in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only).
GateWay Address	xxx.xxx.xxx.xxx	Enter Gateway Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only).
BMC MAC address	xx-xx-xx-xx-xx-xx	Information only.
IPv6 Mode	Disabled* Enabled	Disables/Enables IPv6 internet protocol support.

Remote Access Configuration

Figure 2-22. Remote Access Configuration Screen



Screen

Menu Fields	Settings	Comments
Server/Remote Access Configuration		
Remote Access	Disabled Enabled*	The settings specify how the host computer and the remote system exchanges data. Both systems should have the same or compatible settings.
Serial Port Number	COM1 COM2 as SOL*	Serial port number.
Serial Port Address	3F8h/2F8h* 2F8h/3F8h	COM1/COM2 IO port address.

Menu Fields	Settings	Comments
Serial Port Mode	115200 8-n-1 *	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
	57600 8-n-1	
	38400 8-n-1	
	19200 8-n-1	
	9600 8-n-1	
Flow Control	None*	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
	Hardware	
Redirection After BIOS POST	Disabled Always*	Redirection After BIOS POST
Terminal Type	ANSI*	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
	VT100	
	VT-UTF8	
VT-UTF8 Combo Key Support	Disabled	Enable VT-UTF8 combination key support for ANSI/VT100 terminals.
	Enabled*	

NOTE: BIOS setup screens display at 100 (columns) x 31 (lines). Change the client-side console utility settings to support 100 (columns) x 31 (lines) for accurate screen display.

View System Event Log

Figure 2-23. View System Event Log Screen

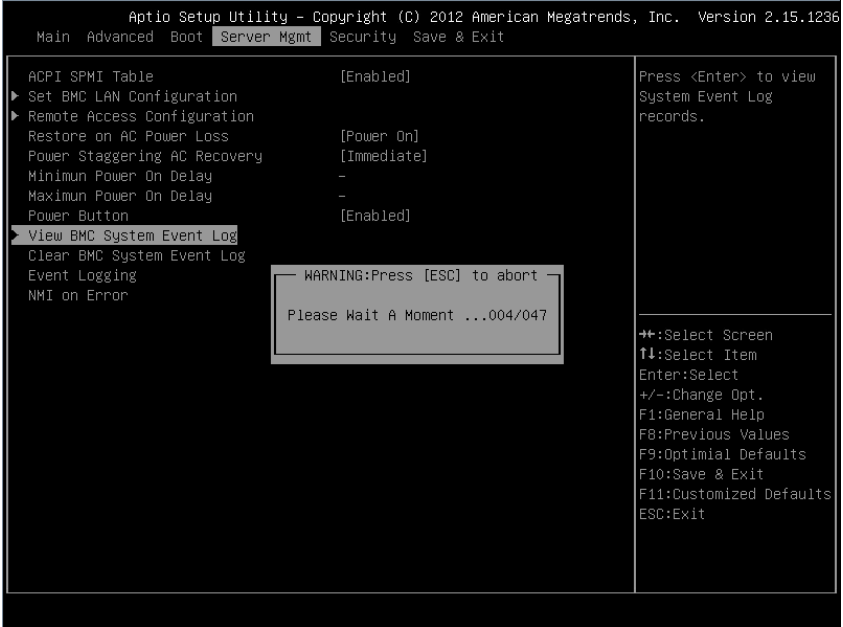


Figure 2-24. View System Event Log Screen *Continued*

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Version 2.15.1236
Server Mgmt

ID	TYPE	DATE	TIME	SENSOR	TYPE
1	02	01/01/70	00:00:40	System	Event
2	02	07/29/13	12:58:11	System	Event
3	02	07/29/13	12:59:00	System	Event
4	02	07/29/13	12:59:09	System	Event
5	02	07/29/13	12:59:47	System	Event
6	02	07/29/13	12:59:52	Power	Unit
7	02	07/29/13	12:59:53	Power	Unit
8	02	01/01/70	00:34:02	System	Event
9	02	07/29/13	14:42:10	System	Event
10	02	07/29/13	14:50:13	System	Event
11	02	07/29/13	14:50:25	System	Event
12	02	07/29/13	14:50:29	System	Event
13	02	07/29/13	14:52:50	System	Event
14	02	07/29/13	14:53:09	System	Event
15	02	07/29/13	14:53:12	System	Event
16	02	07/29/13	14:55:28	System	Event
17	02	07/29/13	14:57:29	System	Event
18	02	07/29/13	14:57:32	System	Event
19	02	07/29/13	14:57:51	Power	Unit
20	02	07/29/13	15:00:27	System	Event
21	02	07/29/13	15:00:40	System	Event
22	02	07/29/13	15:00:43	System	Event
23	02	07/29/13	16:12:03	System	Event
24	02	07/29/13	16:12:26	System	Event

↑
+/:Select Screen
↑↓:Select Item
Enter:Select
+/-:Change Opt.
F1:General Help
F8:Previous Values
F9:Optimal Defaults
F10:Save & Exit
F11:Customized Defaults
ESC:Exit
↓



NOTE: Only provides a brief SEL description for the user. If the user needs more detailed information, refer to the BMC Event Log in the Server Health of WebUI.

Security Menu

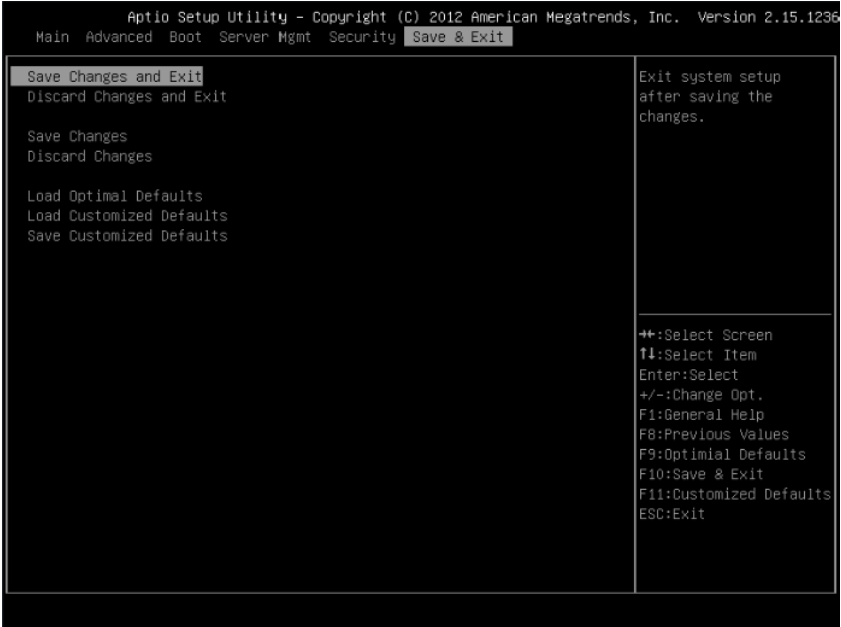
Figure 2-25. Security Menu Screen



Menu Fields	Settings	Comments
Security		
Change Supervisor Password		Set Supervisor Password. While user clear the Supervisor, system will prompt a warning message “Clear Old Password, Continue?”. Both Supervisor and User passwords will be cleared if the user selects “Yes”.
Change User Password		Set User Password.

Save and Exit

Figure 2-26. Save and Exit Screen



Menu Fields	Settings	Comments
Save & Exit		
Save Change and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes		Save Changes done so far to any of the setup option.
Discard Changes		Discard changes done so far to any of the setup option.

Menu Fields	Settings	Comments
Load Optimal Defaults		Restore/Load Default values for all the setup options.
Load Customized Defaults		Restore the User Defaults to all the setup option.
Save Customized Defaults		Save the changes done so far as User Defaults.

Error Handling

This chapter defines the following error handling features:

- Error Handling and Logging
- Error Messages and error code

Error Handling and Logging

This section defines how errors are handled by the system BIOS, including a discussion of the role of the BIOS in error handling and the interaction between the BIOS, platform hardware, and server management firmware with regard to error handling. In addition, error-logging techniques are described.

Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors that can be enabled and disabled individually or as a group can be categorized as follows:

- PCI Express bus error
- Memory single- and multi-bit errors
- Errors detected during POST, logged as POST errors

Sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and logging system events. For more information on BMC logged errors, see the BMC Specification.

Error Logging via SMI Handler

The SMI handler is used to handle and log system level events that are not visible to the server management firmware. The SMI handler pre-processes all system errors, even those that are normally considered to generate an NMI.

The SMI handler sends a command to the BMC to log the event and provides the data to be logged. For example, the BIOS programs the hardware to generate an SMI on a single-bit memory error and logs the DIMM number into the system event log. After BIOS finishes logging the error into BMC, it will assert the NMI if needed.

PCI Express* Errors

The hardware is programmed to generate an SMI on PCIe correctable, uncorrectable non-fatal, and uncorrectable fatal errors. The correctable PCIe errors are reported to the BMC as PCIe Bus Correctable errors. PCIe non-fatal and fatal errors are reported to the BMC as PCIe Bus Uncorrectable errors. The system event log for these errors includes the location of the device reporting an error which includes the PCIe link number, PCI bus number, PCI device number, and the PCI function number. An NMI is generated for PCIe Uncorrectable errors after they are logged.

Processor Bus Error

The BIOS enables the error correction and detection capabilities of the processors by setting appropriate bits in the processor model specific register (MSR) and the appropriate bits inside the chipset.

In the case of unrecoverable errors on the host processor bus, proper execution of the asynchronous error handler (usually SMI) cannot be guaranteed and the handler cannot be relied upon to log such conditions. The handler records the error to the system event log only if the system has not experienced a catastrophic failure that compromises the integrity of the handler.

Memory Bus Error

The hardware is programmed to generate an SMI on correctable data errors in the memory array. The SMI handler records the error and the DIMM location to the system event log. Uncorrectable errors in the memory array are mapped to the SMI because the BMC cannot determine the location of the bad DIMM. The uncorrectable errors may have corrupted the contents of SMRAM. The SMI handler will log the failing DIMM number to the BMC if the SMRAM contents are still valid. The ability to isolate the failure down to a single DIMM may not be available on certain errors, and / or during early POST.

Boot Event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event. Software that parses the event log should not treat the boot event as an error.

Table 2-1. POST Error Events

Byte	Field	Value	Description
1:2	Record ID	XXXXh	ID Used for SEL Record access
3	Record Type	02h	02h = system event record
4:7	Time Stamp	XXXXXXXXh	Time when event was logged
8:9	Generator ID	0100h	Generate by BIOS
10	EvM Rev	04h	Event Message Format Revision. 04h for this specification
11	Sensor Type	0Fh	Sensor type code for sensor that generated the event
12	Sensor Number	DAh	Number of Sensor that generated the event
13	Event Dir Event Type	00h	Bit 7 0 = Assert Event Bit 6:0 Event Type Code
14	Event Data 1	A0h	Bit 7:6 10b = LSB POST error code in byte 2 Bit 5:4 10b = MSB POST error code in byte 3 Bit 3:0 Offset from Event/Reading Code for discrete event status
15	Event Data 2	XXh	POST error code, LSB
16	Event Data 3	XXh	POST error code, LSB

Logging Format Conventions

The BIOS complies with the logging format defined in the IPMI specification. IPMI requires the use of all but two bytes in each event log entry, called Event Data 2 and Event Data 3. An event generator can specify that these bytes contain OEM-specified values. The system BIOS uses these two bytes to record additional information about the error.

This specification describes the format of the OEM data bytes (Event Data 2 and 3) for the following errors:

- Memory errors
- PCI Express bus errors

Event Data 2 and 3 are undefined for all other events that are logged by the BIOS.

The system BIOS sensors are logical entities that generate events. The BIOS ensures that each combination of sensor type (such as memory) and event type (sensor-specific) has a unique sensor number.

Memory Error Events

Table 2-2. Memory Error Events

Byte	Field	Value	Description
01:02	Record ID	XXXXh	ID Used for SEL Record access
3	Record Type	02h	02h = system event record
04:07	Time Stamp	XXXXXXXXh	Time when event was logged
08:09	Generator ID	0100h	Generated by BIOS
10	EvM Rev	04h	Event Message Format Revision. 04h for this specification
11	Sensor Type	0Ch	Sensor type code for sensor that generated the event
12	Sensor Number	7A/7B/7C/7Dh	Number of Sensor that generator the event DIMM A1:7Ah DIMM A0:7Bh DIMM B1:7Ch DIMM B0:7Dh
13	Event Dir Event Type	6Fh	Bit 7 0 = Assert Event Bit 6:0 Event Type Code
14	Event Data 1	0A0h	Bit 7:6 10b = OEM code in byte 2 Bit 5:4 10b = OEM code in byte 3 Bit 3:0 Offset from Event/Reading Code for discrete event status 0h Correctable Error 1h Uncorrectable Error 5h Correctable ECC error logging limit reached.

Table 2-2. Memory Error Events

15	Event Data 2	XXh	(1) 00h: SBE warning threshold (Event/Reading Type Code = 0h for Correctable Error) if supported. (2) 01h: SBE critical threshold (Event/Reading Type Code = 5h for Correctable ECC error logging limit reached) if supported. (3) 0FFh: unspecified (4) other: reserved
16	Event Data 3	XXh	Bit 7:0 Reserved

PCI Express Error Events

Table 2-3. PCI Express Error Events

Byte	Field	Value	Description
1:2	Record ID	XXXXh	ID Used for SEL Record access
3	Record Type	02h	02h = system event record
4:7	Time Stamp	XXXXXXXXh	Time when event was logged
8:9	Generator ID	0100h	Generated by BIOS
10	EvM Rev	04h	Event Message Format Revision. 04h for this specification.
11	Sensor Type	13h	Sensor type code for sensor that generated the event.
12	Sensor Number	7AE3h	Number of Sensor that generated the event.
13	Event Dir Event Type	6Fh	Bit 7 0 = Assert Event Bit 6:0 Event Type Code
14	Event Data 1	AXh	Bit 7:6 10b = OEM code in byte 2 Bit 5:4 10b = OEM code in byte 3 Bit 3:0 Offset from Event/Reading Code for discrete event status 7h Bus Correctable Error (NFERR) 8h Bus Uncorrectable Error (NFERR) Ah Bus Fatal (FERR)
15	Event Data 2	XXh	Bit 7:3 Device Number Bit 2:0 Function Number
16	Event Data 3	XXh	Bit 7:0 Reserved

Error Messages and Handling

The system BIOS displays error messages on the video screen. When system can't detect any USB Keyboard or BIOS setting is reset, BIOS will display error messages on the screen. Users could enable the Pause on Error function in BIOS setup menu in order to make the system pause on the error message

screen.

Table 2-4. POST Error Messages and Handling

Error Message	Solution
No USB Keyboard!	System can't detect any USB Keyboard. Please plug in an USB keyboard
CMOS Battery Failed!	BIOS setting is reset. Please adjust BIOS setting yourself.

Aptio Checkpoints

Checkpoint Ranges

Table 2-5. Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

Standard Checkpoints

SEC Phase

Table 2-6. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Table 2-7. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection

Table 2-7. PEI Phase (continued)

Status Code	Description
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)

Table 2-7. PEI Phase (continued)

Status Code	Description
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost

Table 2-7. PEI Phase (continued)

Status Code	Description
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Table 2-8. DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization

Table 2-8. DXE Phase (continued)

Status Code	Description
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization

Table 2-8. DXE Phase (continued)

Status Code	Description
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin

Table 2-8. DXE Phase (continued)

Status Code	Description
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed

Table 2-8. DXE Phase (continued)

Status Code	Description
0xDC	Reset protocol is not available

PEI Beep Codes

Table 2-9. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXE IPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

DXE Beep Codes

Table 2-10. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available

Table 2-10. DXE Beep Codes (continued)

# of Beeps	Description
8	Platform PCI resource requirements cannot be met

ACPI/ASL Checkpoints**Table 2-11. ACPI/ASL Checkpoints**

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Checkpoint Ranges**Table 2-12. OEM Reserved Checkpoint Ranges**

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes

Table 2-12. OEM Reserved Checkpoint Ranges (continued)

Status Code	Description
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Intel Memory Reference Code Checkpoints

The BIOS will show MRC error/warning codes on the 80port LED when MRC errors happen. The LED flash sequence will be (with 1 second interval):

- For no specific DIMM location errors (ex. no memory detected):
- "Major error code" -> "Minor error code" -> "0" -> ... (repeat)
- For specific DIMM location errors (ex. wrong DIMM population):
- "Major error code" -> "Minor error code" -> "DIMM location" -> "0" -> ... (repeat)

Table 2-13. MRC DIMM to Error Code Mapping

Node	Channel	DIMM	Error Code
0	0	0	0xA0
0	0	1	0xA1
0	1	0	0xA2
0	1	1	0xA3

Table 2-14. MRC POST Code

POST Code Nomenclature	Major Code	Minor Code	Description
STS_DIMM_DETECT	B0h		Detect DIMM population
STS_CLOCK_INIT	B1h		Set DDR3 frequency
STS_SPD_DATA	B2h		Gather remaining SPD data
STS_GLOBAL_EARLY	B3h		Program registers on the memory controller level
STS_RANK_DETECT	B4h		Evaluate RAS modes and save rank information
STS_CHANNEL_EARLY	B5h		Program registers on the channel level
STS_JEDEC_INIT	B6h		Perform the JEDEC defined initialization sequence
STS_CHANNEL_TRAINING	B7h		Train DDR3 ranks
STS_RD_DQS		01h	Read DQ/DQS training

POST Code Nomenclature	Major Code	Minor Code	Description
STS_REC_EN		02h	Receive Enable training
STS_WR_LVL		03h	Write Leveling training
STS_WR_DQS		04h	Write DQ/DQS training
STS_INIT_DONE		05h	DDR channel training done
STS_INIT_THROTTLING	B8h		Initialize CLTT/OLTT
STS_MEMBIST	B9h		Hardware memory test and init
STS_SOFT_INIT	BAh		Execute software memory init
STS_DDR_MEMMAP	BBh		Program memory map and interleaving
STS_RAS_CONFIG	BCh		Program RAS configuration
STS_MRC_DONE	BFh		MRC is done

Table 2-15. MRC Fatal Error Code

POST Code Nomenclature	Major Code	Code Minor	Description
ERR_NO_MEMORY	0E8h		

Table 2-15. MRC Fatal Error Code (continued)

POST Code Nomenclature	Major Code	Code Minor	Description
ERR_NO_MEMORY_MINOR_NO_MEMORY		01h	1. No memory was detected via SPD read. No warning log entries available. 2. Invalid config that causes no operable memory. Refer to warning log entries for details.
ERR_NO_MEMORY_MINOR_ALL_CH_DISABLED		02h	Memory on all channels of all sockets are disabled due to hardware memtest error
ERR_NO_MEMORY_MINOR_ALL_CH_DISABLED_MIXED		03h	No memory installed. All channels are disabled.
ERR_LT_LOCK	0E9h		Memory is locked by LT, inaccessible.
ERR_DDR_INIT	0EAh		DDR3 training did complete successfully
ERR_RD_DQ_DQS		01h	Error on read DQ/DQS init
ERR_RC_EN		02h	Error on Receive Enable
ERR_WR_LEVEL		03h	Error on Write Leveling
ERR_WR_DQ_DQS		04h	Error on write DQ/DQS
ERR_MEM_TEST	0EBh		Memory test failure

Table 2-15. MRC Fatal Error Code (continued)

POST Code Nomenclature	Major Code	Code Minor	Description
ERR_MEM_TEST_MINOR_SOFTWARE		01h	Software memtest failure
ERR_MEM_TEST_MINOR_HARDWARE		02h	Hardware memtest failed
ERR_MEM_TEST_MINOR_LOCKSTEP_MODE		03h	Hardware Memtest failure in Lockstep Channel mode requiring a channel to be disabled. This is a fatal error which requires a reset and calling MRC with a different RAS mode to retry.
ERR_VENDOR_SPECIFIC	0ECh		
ERR_DIMM_COMPAT	0EDh		UDIMMs and RDIMMs are both present DIMM vendor-specific errors
ERR_MIXED_MEM_TYPE		01h	Different dimm types are detected installed in the system
ERR_INVALID_POP		02h	Violation of population rules
ERR_INVALID_POP_MINOR_QR_AND_3RD_SLOT		03h	The 3rd DIMM slot can not be populated when QR DIMMs are installed
ERR_INVALID_POP_MINOR_UDIMM_AND_3RD_SLOT		04h	UDIMMs and SODIMMs are not supported in the third DIMM slot
ERR_INVALID_POP_MINOR_UNSUPPORTED_VOLTAGE		05h	Unsupported DIMM Voltage

Table 2-15. MRC Fatal Error Code (continued)

POST Code Nomenclature	Major Code	Code Minor	Description
ERR_MRC_STRUCT	0EFh		Indicates a CLTT table structure error. A DIMM is populated in the 3rd slot when quad rank DIMM is present in the channel.
ERR_INVALID_BOOT_MODE		01h	Boot mode is unknown
ERR_INVALID_SUB_BOOT_MODE		02h	Sub boot mode is unknown

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_RDIMM_ON_UDIMM	01h		NOD E	CH	DIMM	X	RDIMM is plugged into a UDIMM only board
WARN_UDIMM_ON_RDIMM	02h		NOD E	CH	DIMM	X	UDIMM is plugged into a RDIMM only board
WARN_SODIMM_ON_RDIMM	03h						No current use (TBD)
WARN_4Gb_FUSE	04h		NOD E	CH	DIMM	X	Support for 4Gb devices has been fused off
WARN_8Gb_FUSE	05h		NOD E	CH	DIMM	X	Support for 8Gb devices has been fused off

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_IMC_DISABLED	06h						Not in use (TBD)
WARN_DIMM_COMPAT	07h		NODE	CH	DIMM	X	DIMM is not compatible with the IMC memory controller.
WARN_DIMM_COMPAT_MINOR_X16_COMBO		01h	NODE	CH	DIMM	X	x16 UDIMM found on a combo board that supports both RDIMM and UDIMM. MRC has disabled this entire channel.
WARN_DIMM_COMPAT_MINOR_MAX_RANKS		02h	NODE	CH	DIMM	X	Max number of ranks exceeded on the channel. MRC has disabled this entire channel.
WARN_DIMM_COMPAT_MINOR_QR		03h	NODE	CH	DIMM	X	QR DIMM is not at Slot0 while SR/DR DIMMs are present in the channel. MRC has disabled this entire channel.
WARN_DIMM_COMPAT_MINOR_NOT_SUPPORTED		04h	NODE	CH	DIMM	X	Incompatible DDR3 DIMM module (type/org/tech/speed etc. not supported). MRC has disabled this entire channel.

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_RANK_NUM		05h	NOD E	CH	DIMM	X	The number of ranks on this device is not supported
WARN_TOO_SLOW		06h	NOD E	CH	DIMM	X	This DIMM does not support DDR3-800 or higher
WARN_DIMM_COMPAT_MINOR_ROW_ADDR_ORDER		07h	NOD E	CH	DIMM	X	LRDIMM A16 usage is not symmetrical on channel for JKT Astep
WARN_LOCK_STEP_DISABLE	09h		X	X	X	X	Lockstep Channel mode was requested but could not be honored
WARN_LOCKS_TEP_DISABLE_MINOR_RAS_MODE		01h	X	X	X	X	Unable to enable Lockstep mode because ECC is disabled. Switch to independent channel mode. (2)
		02h					
WARN_LOCK_STEP_DISABLE_MINOR_MEM_TEST_FAILED		03h					TBD: not currently in use.

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_USER_DIMM_DISABLE	0Ah		NODE	CH	X	X	DIMM was disabled by MRC. See minor code below for specific reasons.
WARN_USER_DIMM_DISABLE_QUAD_AND_3DPC		01h	NODE	CH	X	X	3-DIMM-Per-Channel and <u>Qu</u> ak Rank DIMM were found on the same CPU socket (unsupported config). Channel with <u>Qu</u> ad Rank DIMM is disabled by MRC.
WARN_USER_DIMM_DISABLE_MEMTEST		02h	NODE	CH	X	X	DIMM was disabled by the MRC as a result of previous DIMM in the channel being disabled due to error (the DIMM itself is not necessarily bad)
WARN_MEMTEST_DIMM_DISABLE	0Bh		NODE	CH	DIMM	X	DIMM was disabled due to MemTest errors.
WARN_MIRROR_DISABLE	0Ch		X	X	X	X	Mirror mode was requested but could not be honored. Memtest failure resulted in a channel being disabled. Switch to independent channel mode.

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_MIRROR_DISABLE_MINOR_RAS_DISABLED		01h	X	X	X	X	Unable to enable Mirror mode because ECC is disabled. Switch to independent channel mode. (2)
WARN_MIRROR_DISABLE_MINOR_MISMATCH		02h	X	X	X	X	Mismatched DIMM pairs found across channels. Switch to independent channel mode.
WARN_MIRROR_DISABLE_MINOR_MEMTEST		03h	X	X	X	X	Mirror mode was disabled due to memory test failure
WARN_MEM_LIMIT	0Dh		X	X	X	X	IMC memory decode limit was reached before all memory could be allocated.
WARN_INTERLEAVE_FAILURE	0Eh						Interleave mode failure
WARN_SAD_RULES_EXCEEDED		01h	X	X	X	X	Number of SAD rules exceeds
WARN_TAD_RULES_EXCEEDED		02h	NODE	X	X	X	Number of TAD rules exceeds
WARN_RIR_RULES_EXCEEDED		03h	NODE	CH	X	X	Number of RIR rules exceeds
WARN_TAD_OFFSET_NEGATIVE		04h	NODE	X	X	X	Negative TAD offset

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_TAD_LIMIT_ERROR		05h	NODE	X	X	X	TAD Limit > SAD Limit
WARN_SPARE_DISABLE	10h		X	X	X	X	Unable to enable Spare mode because ECC is disabled. Switch to independent channel mode. (2) Mismatched IMM pairs found across channels. Switch to independent channel mode.
WARN_PTRLSCRB_DISABLE	11h						TBD: not currently in use.
WARN_UNUSED_MEMORY	12h		NODE	CH	X	X	Unused memory is populated on channel 2 in Lockstep or Mirroring mode.
WARN_UNUSED_MEMORY_MIRROR		01h	NODE	2	X	X	Unused memory is populated on channel 2 in mirror mode
WARN_UNUSED_MEMORY_LOCKSTEP		02h	NODE	2	X	X	Unused memory is populated on channel 2 in Lockstep mode

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_RD_DQ_DQS	13h		NODE	CH	DIMM	X	A Read DQ/DQS failure has occurred during training. The failing Channel was disabled
WARN_RD_RCVEN	14h		NODE	CH	X	X	A tRLCoarse failure has occurred during DDR training. The failing Channel was disabled.
WARN_ROUNDTRIP_EXCEEDED		01h	NODE	CH	DIMM	RANK	Round Trip delay of %d exceeds the limit of %d
WARN_WR_LEVEL	15h		NODE	CH	DIMM	X	A write leveling failure has occurred during training.
WARN_WR_FLYBY		01h	NODE	CH	X	X	Fault Parts Tracking write Fly-by error
WARN_WR_DQ_DQS	16h		NODE	CH	DIMM	X	A write DQ/DQS failure has occurred during training.
WARN_DIMM_POP_RULE	17h		NODE	CH	DIMM	X	Improper DIMM population

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_DIMM_POP_RULE_MINOR_OUT_OF_ORDER		01h	NODE	CH	DIMM	X	DIMM is populated out of order and that it will not be used. If slot 0 is empty then the channel gets disabled, if slot 1 is empty but slot 0 and slot 2 are populated then MRC will try to boot with the DIMM in slot 0 while ignoring the DIMM in slot 2.
WARN_DIMM_POP_RULE_MINOR_INDEPENDENT_MODE		02h	NODE	2	X	X	Lockstep/Mirror mode not enabled due to unused DIMM on Channel 2, and MRC input RAS_TO_INDP_EN = 1. Switch to Independent Channel mode.
WARN_CLTT_DISABLE	18h						CLTT was requested but could not be honored

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_CLTT_MINOR_NO_TEMP_SENSOR		01h	NODE	CH	DIMM	X	A DIMM without Temp Sensor was found
WARN_CLTT_MINOR_CIRCUIT_TST_FAILED		02h	NODE	CH	DIMM	X	A DIMM failed Temp Sensor circuit test
WARN_THROT_INSUFFICIENT	19h		NODE	CH	DIMM	X	Indicates throttling is not sufficient for this DIMM due to MRC calculation.
WARN_CLTT_DIMM_UNKNOWN	1Ah		NODE	CH	DIMM	X	A DIMM of an unknown category is found when looking up a predefined category table (DIMM type, rawcard, heat spreader, planner, etc). Use a default category (category 11 or 27 depending on DIMM type)
WARN_DQS_TEST	1Bh		X	X	X	X	DQS training failure encountered
WARN_MEMTEST	1Ch		NODE	CH	DIMM	X	Hardware Memtest failed and the DIMM is disabled
WARN_CLOSED_PAGE_OVERRIDE	1Dh						TBD: not currently in use.

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_DIMM_VREF_NOT_PRESENT	1Eh		NODE	X	X	X	DIMM Verf controller circuit (DCP) not detected
WARN_LV_STD_DIMM_MIX	20h		NODE	X	X	X	Low voltage DDR3 problem encountered.
WARN_LV_2QR_DIMM	21h						TBD: not currently in use.
WARN_LV_3DPC	22h						TBD: not currently in use.
WARN_FPT_CORRECTABLE_ERROR	30h						FTP correctable error
WARN_FPT_MINOR_READ_DQ_DQS		13h	NODE	CH	DIMM	RANK	FTP: failed Read DqDqs
WARN_FPT_MINOR_READ_RCVEN		14h	NODE	CH	DIMM	RANK	failed Receive Enable
WARN_FPT_MINOR_WRITE_LEVEL		15h	NODE	CH	DIMM	RANK	FTP: failed Write Levelling
WARN_FPT_MINOR_WRITE_FLYBY		00h					TBD: not currently used
WARN_FPT_MINOR_WRITE_DQ_DQS		16h	NODE	CH	DIMM	RANK	FTP: failed Write DqDqs
WARN_FPT_MINOR_WRITE_DQS_TEST		1Bh					TBD: not currently used

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_FPT_MINO R_M EM_TEST		1Ch	NODE	CH	DIMM	RANK	FTP minor correctable memtest WARN_FPT_UNCORRE
CTABLE_ERROR	31h						FTP uncorrectable error
WARN_FPT_MINO R_RD_DQ_DQS		13h	NODE	CH	DIMM	RANK	FTP: failed Read DqDqs
WARN_FPT_MINO R_R D_RCVEN		14h	NODE	CH	DIMM	RANK	Receive Enable training failure
WARN_FPT_MINO R_W R_LEVEL		15h	NODE	CH	DIMM	RANK	FTP failed Write Levelling
WARN_FPT_MINO R_W R_FLYBY		00h					TBD: not currently used
WARN_FPT_MINO R_W R_DQ_DQS		16h	NODE	CH	DIMM	RANK	FTP: failed Write DqDq
WARN_FPT_MINO R_D QS_TEST		1Bh					TBD: not currently used
WARN_FPT_MINO R_M EM_TEST		1Ch	NODE	CH	DIMM	RANK	FTP minor correctable memtest

Table 2-16. MRC Warning Code

Warning	Major Code	Minor Code	Data (DWord)				Descriptions
	31:16	15:0	31:24	23:16	15:8	7:0	
WARN_MEM_CONFIG_CHANGED	40h		X	X	X	X	Timing overrides are enabled but the DIMM configuration has changed. Memory overrides will be disabled
WARN_MEM_OVERRIDE_DISABLED		01h	X	X	X	X	If MEM_OVERRIDE_EN is enabled but the DIMM configuration has changed, this warning indicates that the MRC has disabled memory overrides.

Command Line Interfaces for Setup options

The SETUP menu provides setup options through the system configuration utility (`syscfg`), included in the Dell OpenManage Deployment Toolkit (DTK).

Users can use the utility as following:

To change the SETUP option thru D4 token:

```
./syscfg -t=D4_token_id
```

Example:

```
./syscfg -t=0x002D to enable NIC1
```

To check token active status:

```
./syscfg --istokenactive=D4_token_id
```

Example:

```
./syscfg --istokenactive=0x002D to check the token active status of NIC1
```

To directly change the SETUP option thru BMC memory:

```
./ipmitool raw <command> <data>
```

Example:

```
./ipmitool raw 0xc 1 1 3 10 106 42 120 to set IP address of BMC LAN port  
as 10.106.42.120
```


Installing System Components

Safety Measures



CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized is not covered by warranty. Read and follow the safety instructions that came with the product.

System components and electronic circuit boards can be damaged by discharges of static electricity. Working on systems that are still connected to a power supply can be extremely dangerous. To avoid injury to yourself or damage to system, follow these guidelines:

- If possible, wear a grounded wrist strap when you are working inside the system chassis. Alternatively, discharge any static electricity by touching the bare metal chassis of the system chassis, or the bare metal body of any other grounded appliance.
- Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Do not flex or stress the circuit board.
- Leave all components inside the static-proof packaging until you are ready to use the component for the installation.

Recommended Tools

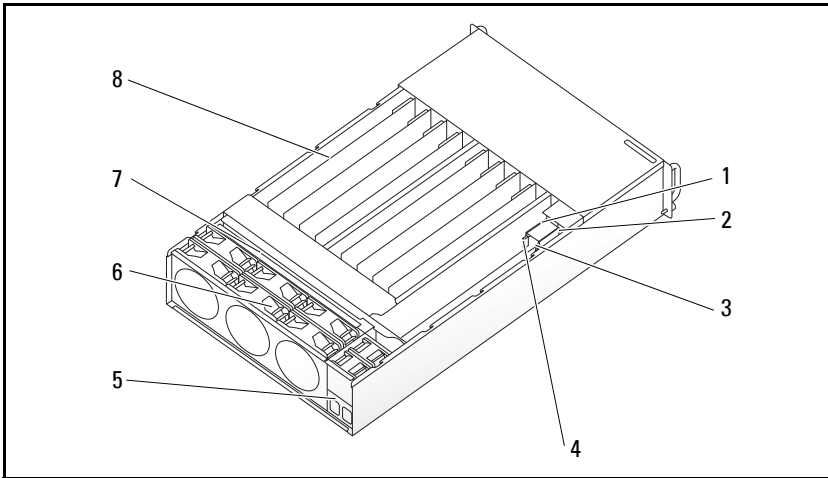
- Phillips screwdriver #2

Inside the System

CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized is not covered by warranty. Read and follow the safety instructions that came with the product.

CAUTION: This system must be operated with the system cover installed to ensure proper cooling.

Figure 3-1. Inside the System



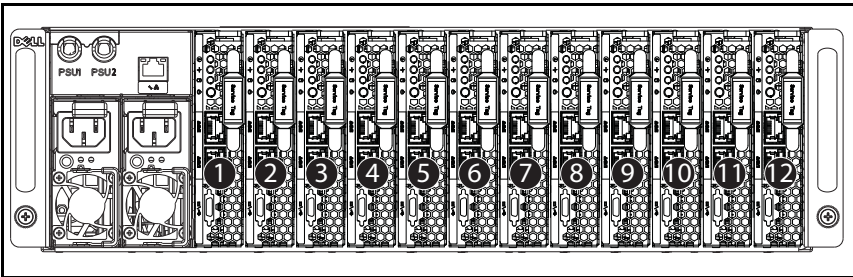
- | | | | |
|---|----------------------|---|------------|
| 1 | PSU 1 | 2 | PSU 2 |
| 3 | PDB 1 | 4 | PDB 2 |
| 5 | power socket bracket | 6 | fan cage |
| 7 | backplane | 8 | sleds (12) |

Sled Configuration

△ CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized by Dell is not covered by your warranty. Read and follow the safety instructions that came with the product.

The following illustrations displays the sled numbering in the system.

Figure 3-2. PowerEdge C5230 12-Sled System



Sleds

Removing a Sled



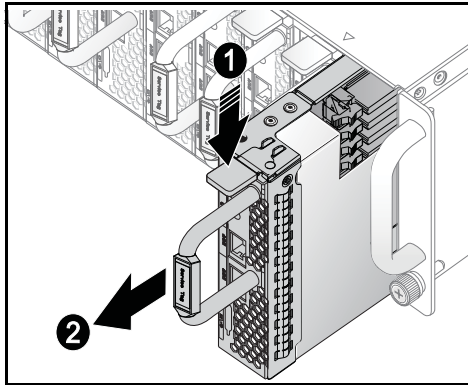
CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized by Dell is not covered by your warranty. Read and follow the safety instructions that came with the product.



CAUTION: To ensure proper airflow in the system, if a sled is removed it should be immediately replaced with another sled or sled dummy.

- 1 Press the release latch down ❶.
- 2 Pull the sled out of the system ❷.

Figure 3-3. Removing a Sled



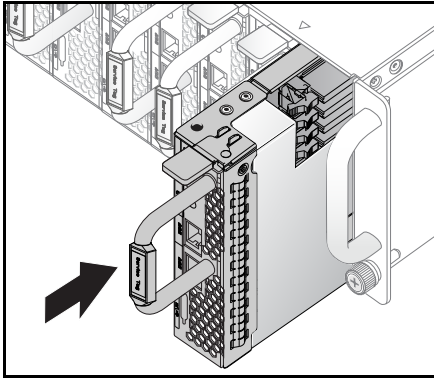
Installing a Sled

△ **CAUTION:** Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized by Dell is not covered by your warranty. Read and follow the safety instructions that came with the product.

△ **CAUTION:** To ensure proper airflow in the system, if a sled is removed it should be immediately replaced with another sled or sled dummy.

Push the sled into the system until flush with the case and the release latch locks

Figure 3-4. Installing a Sled.

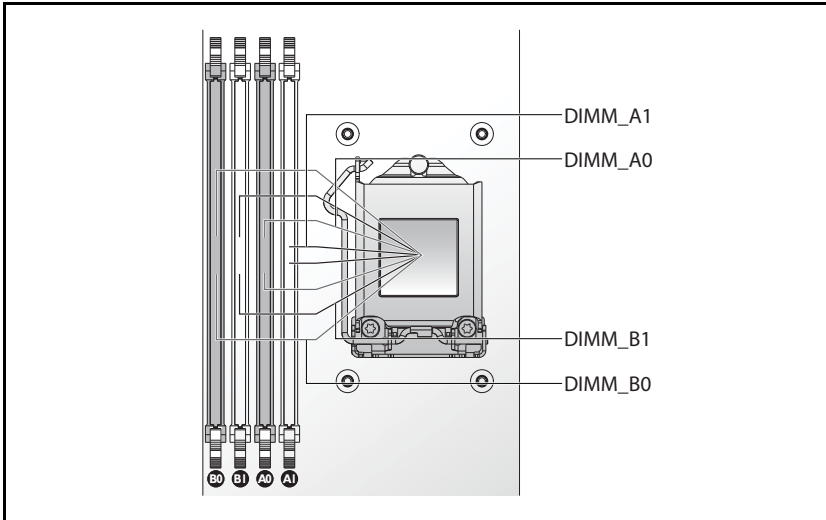


Memory Modules

Supported DIMM Configuration

The following DIMM configurations are supported by the system.

Figure 3-5. DIMM Slot Configuration



DIMM Population Rules

For a single DIMM, only install in DIMM A0.

For two DIMMs, install in DIMM A0 + B0.

Supported Memory



NOTE: Only Intel Xeon E3-1200v3 family of products support 1600 MHz memory.

Supported Memory

Configuration	Memory Type/Size	CPU	DIMMs	Type	Memory Speed (MHz)	Rank	Type (x8, x4)	Component Density	Total Size	DIMM Slot			
										A1	A0	B1	B0
12 sled	DDR3 ECC UDIMM/4096 MB*1	1	1	VLP UDIMM	1600	2R	x8	2GB	4G		•		
12 sled	DDR3 ECC UDIMM/4096 MB*2	1	2	VLP UDIMM	1600	2R	x8	2GB	8G		•		•
12 sled	DDR3 ECC UDIMM/2048 MB*2+4096 MB*3	1	3	VLP UDIMM	1600	2R	x8	2GB	12G	•	•		•
12 sled	DDR3 ECC UDIMM/4096 MB*4	1	4	VLP UDIMM	1600	2R	x8	2GB	16G	•	•	•	•
12 sled	DDR3 ECC UDIMM/8912MB*1	1	1	VLP UDIMM	1600	2R	x8	4GB	8G		•		
12 sled	DDR3 ECC UDIMM/8912MB*2	1	2	VLP UDIMM	1600	2R	x8	4GB	16G		•		•
12 sled	DDR3 ECC UDIMM/8912MB*3	1	3	VLP UDIMM	1600	2R	x8	4GB	24G	•	•		•
12 sled	DDR3 ECC UDIMM/8912MB*4	1	4	VLP UDIMM	1600	2R	x8	4GB	32G	•	•	•	•
12 sled	DDR3 ECC UDIMM/8912MB*2 +4096MB*2	1	4	VLP UDIMM	1600	2R/2R	x8	4GB/2GB	24G	8GB	8G	4G	4G

Removing a Memory Module



WARNING: The memory modules are hot to touch for some time after the system has been powered down. Allow time for the memory modules to cool before handling them. Handle the memory modules by the card edges and avoid touching the components on the memory module.

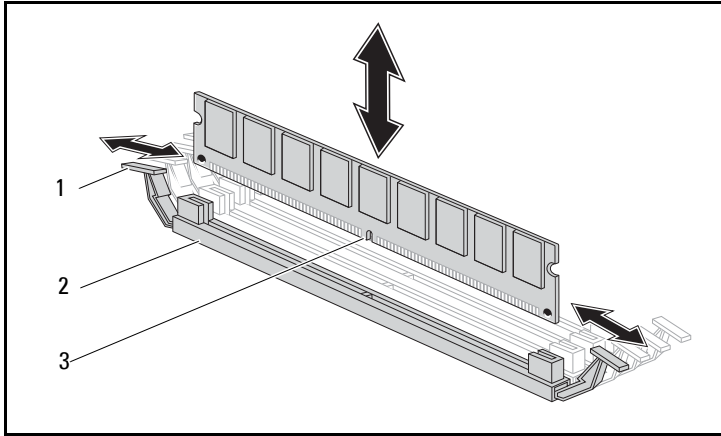


CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized is not covered by warranty. Read and follow the safety instructions that came with the product.

- 1 Remove the sled from the system. See "Removing a Sled" on page 102.

- 2 Push the locking latches of the DIMM slot outwards. See Figure 3-6.
- 3 Remove the memory module from the system.

Figure 3-6. Removing and Installing a Memory Module



- | | | | |
|---|---------------------|---|-----------|
| 1 | locking latch | 2 | DIMM slot |
| 3 | memory module notch | | |

Replacing a Memory Module



WARNING: The memory modules are hot to touch for some time after the system has been powered down. Allow time for the memory modules to cool before handling them. Handle the memory modules by the card edges and avoid touching the components on the memory module.



CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized is not covered by warranty. Read and follow the safety instructions that came with the product.

The system board has four slots in two channels for the installation of memory modules. See "System Board Jumpers and Connectors" on page 137 for the location of the memory modules.

Follow the instructions given below to install memory modules:

- 1 Align the memory module correctly with the DIMM slot. Note the notch and obstruction in Figure 3-6.
- 2 Press the edge connector of the memory module into the DIMM slot. Press down firmly on the memory module so that the locking latches of the DIMM slot are levered upwards to secure the memory module in place.

Hard Drives

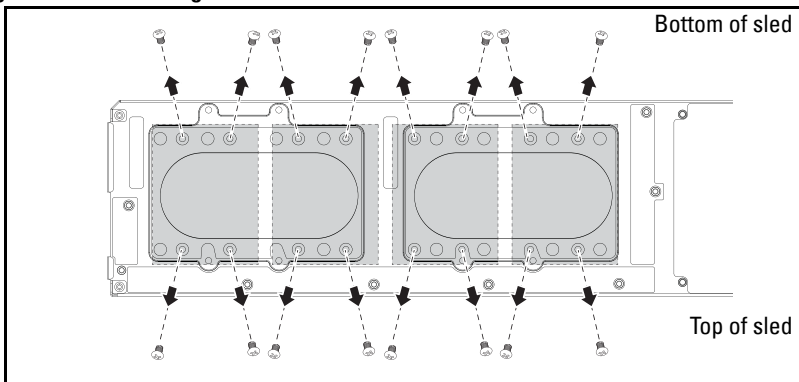
The following are examples showing the installation and removal procedures for the 2.5-inch and the 3.5-inch hard drives.

Removing a 2.5-inch Hard Drive

△ CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized by Dell is not covered by your warranty. Read and follow the safety instructions that came with the product.

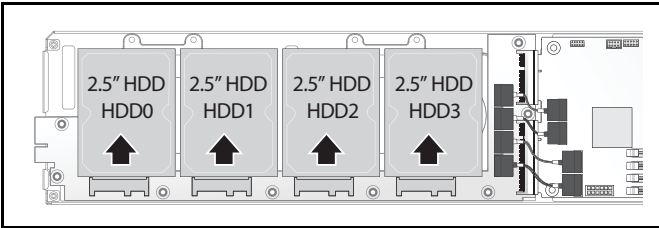
- 1 Remove the sled from the system. See "Sled Configuration" on page 101.
- 2 Remove the hard drive from the sled docking bay.
- 3 Select the hard drive to replace and remove the four hard drive bracket screws securing it underneath the sled.

Figure 3-7. Removing the 2.5" Hard Drive Bracket Screws



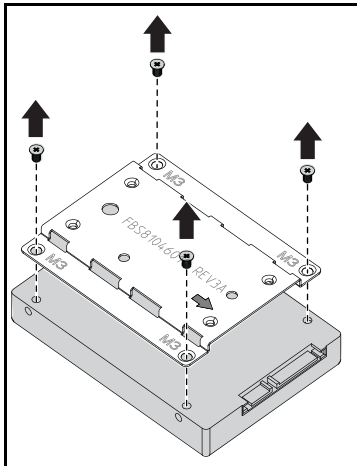
- 4 Remove the hard drive from the sled docking bay.

Figure 3-8. Removing a 2.5" Hard Drive from the Sled



- 5 Remove the four screws from the 2.5-inch hard drive bracket, then detach the hard drive from the bracket.

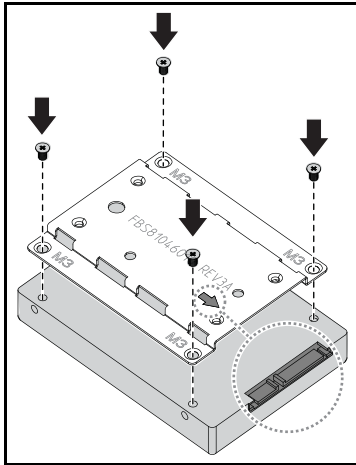
Figure 3-9. Separating the 2.5" Hard Drive Bracket from the Hard Drive.




Installing a 2.5-inch Hard Drive

- 1 Align the 2.5-inch hard drive bracket on the new hard drive then replace the four screws.

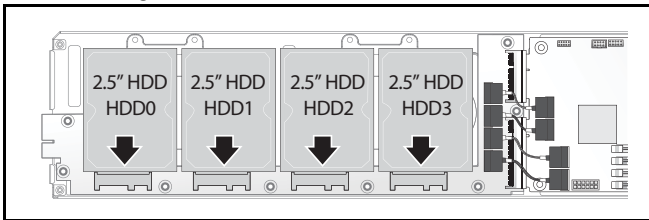
Figure 3-10. Aligning the 2.5" Hard Drive Bracket



 **NOTE:** The correct orientation of the bracket is with the arrow mark pointing towards the hard drive connector.

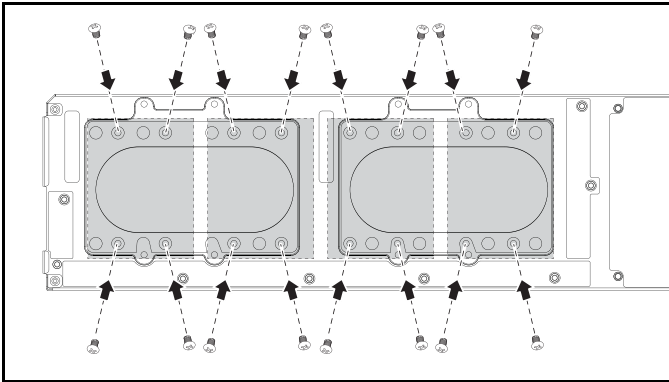
- 2 Connect the hard drive to the hard drive board in the sled.

Figure 3-11. Connecting the 2.5" Hard Drive to the Hard Drive Board



- 3 Replace the sled hard drive bracket screws underneath the sled.

Figure 3-12. Securing the 2.5" Hard Drive Bracket

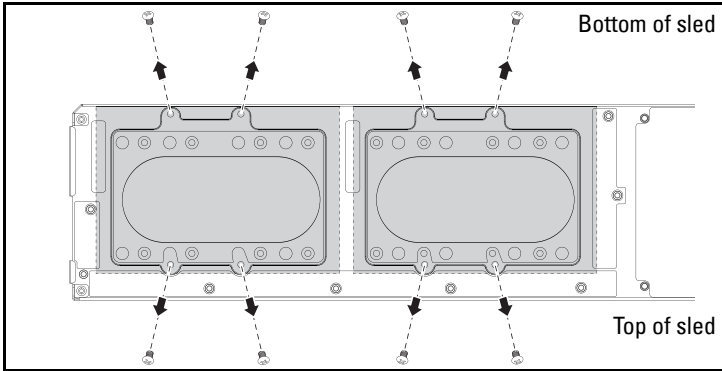


Removing a 3.5-inch Hard Drive

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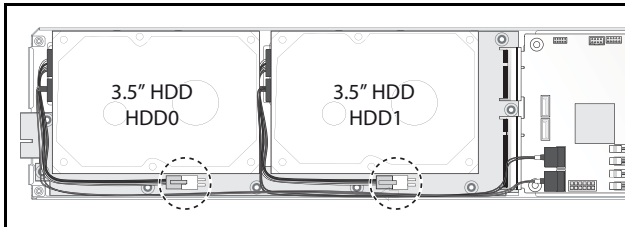
- 1 Remove the sled from the system. See "Removing a Sled" on page 102.
- 2 Remove the hard drive bracket screws from underneath the sled.

Figure 3-13. Removing the 3.5" Hard Drive Bracket Screws



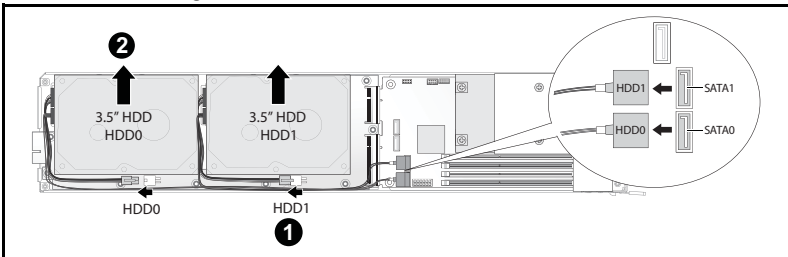
- 3 Remove the hard drive cables from the cable clips.

Figure 3-14. Disconnecting the 3.5" Hard Drive Cables from the Board



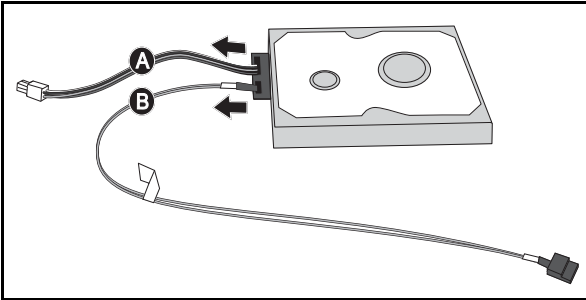
- 4 Disconnect the hard drive cables from the hard drive board and system board ❶ then lift the hard drive out of the sled ❷.

Figure 3-15. Removing the 3.5" Hard Drives from the Sled



- 5 Disconnect the hard drive cables A and B from the hard drive.

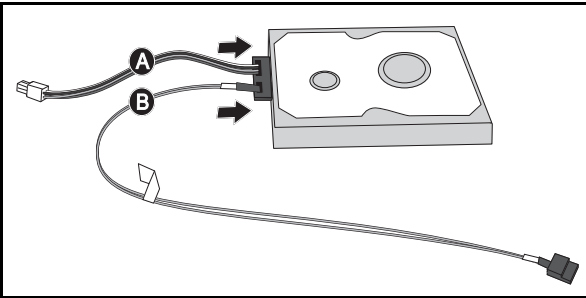
Figure 3-16. Disconnecting the Hard Drive Cables from the Hard Drive



Installing a 3.5-inch Hard Drive

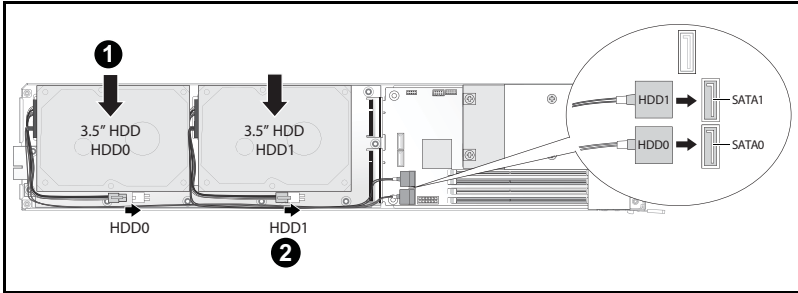
- 1 Connect the hard drive cables A and B to a new hard drive.

Figure 3-17. Connecting the Cables to the Hard Drive



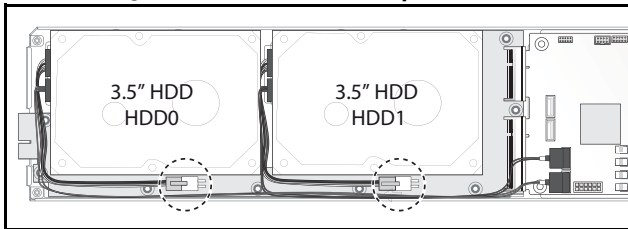
- 2 Place the hard drive in the sled ❶ then connect the hard drive cables to the hard drive board and system board ❷.

Figure 3-18. Installing the Hard Drives in the Sled



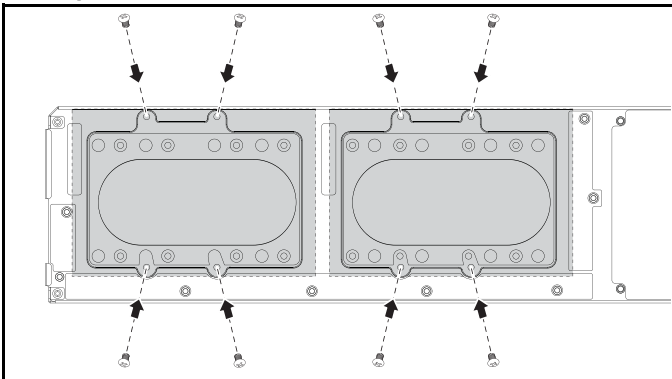
- 3 Insert the hard drive cables into the cable clips.

Figure 3-19. Connecting the Cables in the Cable Clips



- 4 Replace the hard drive bracket screws underneath the sled.

Figure 3-20. Replacing the Bracket Screws in the Sled



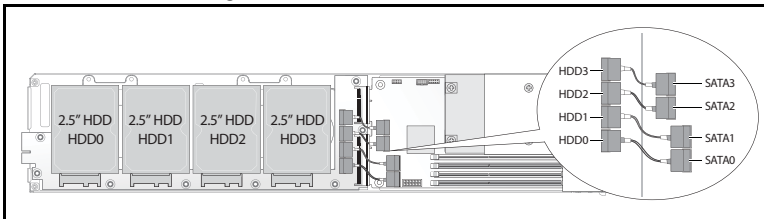
Hard Drive Boards

Removing a 2.5-inch Hard Drive Board

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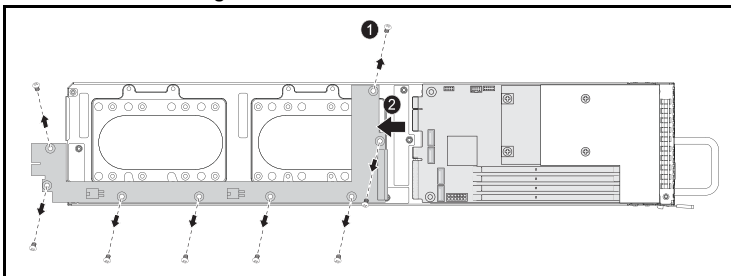
- 1 Remove the hard disks. See "Hard Drives" on page 109.
- 2 Disconnect the four SATA cables between the hard drive board and the system board.

Figure 3-21. Disconnecting the SATA Cables



- 3 Remove the eight screws from the hard drive board ①.
- 4 Disconnect the hard drive board from the system board ② and lift out of the sled.

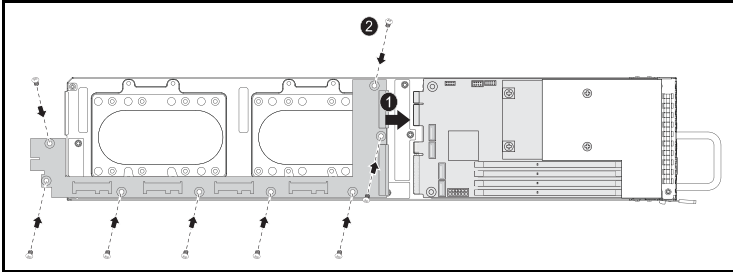
Figure 3-22. Disconnecting the 2.5" Hard Drive Board



Installing a 2.5-inch Hard Drive Board

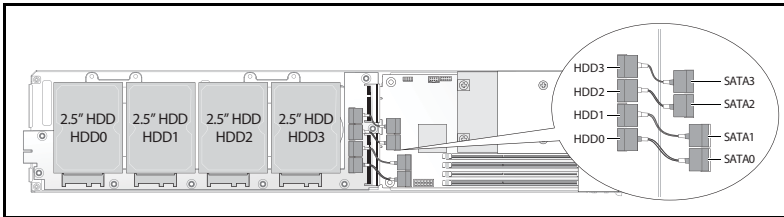
- 1 Holding the board by the edges, place the hard drive board into the sled and connect to the system board ❶.
- 2 Replace the eight screws to secure it in place ❷.

Figure 3-23. Securing the 2.5" Hard Drive Board



- 3 Connect the four SATA cables between the hard drive board and the system board.

Figure 3-24. Connecting the SATA Cables



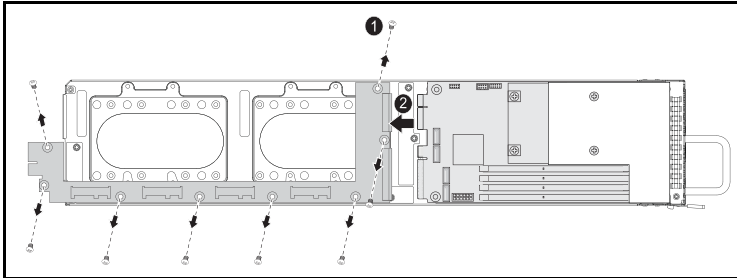
Removing a 3.5-inch Hard Drive Board

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- 1 Remove the hard drives. See "Removing a 3.5-inch Hard Drive" on page 112.
- 2 Remove the eight screws from the hard drive board ❶.

- 3 Disconnect the hard drive board from the system board ② and lift out of the sled.

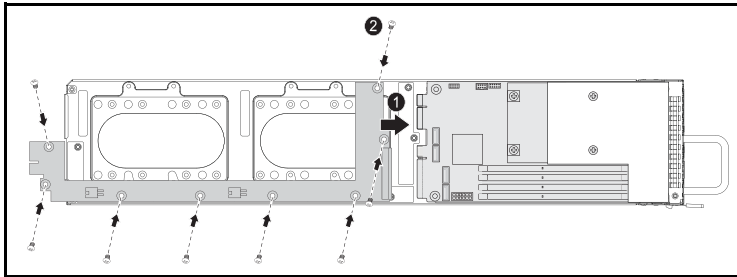
Figure 3-25. Disconnecting the 3.5" Hard Drive Board



Installing a 3.5-inch Hard Drive Board

- 1 Unpack the new hard drive board.
- 2 Holding the board by the edges, place the hard drive board into the sled and connect to the system board ①.
- 3 Replace the eight screws to secure it in place ②.

Figure 3-26. Installing a 3.5" Hard Drive Board



Heat Sinks

The following procedures illustrate removal and installation of the heat sink/shroud.


Table 3-1. Processors Requiring a Heat Sink/Shroud

Series	Processor
Intel Xeon E3-1200v3 product family	Intel Xeon E3-1280v3 Intel Xeon E3-1240v3

Removing a Heat Sink/Shroud

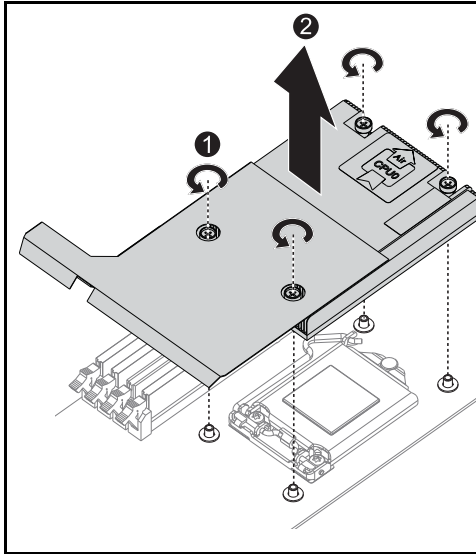


CAUTION: Many repairs may only be done by a certified service technician. You should only perform troubleshooting and simple repairs as authorized in your product documentation, or as directed by the online or telephone service and support team. Damage due to servicing that is not authorized by Dell is not covered by your warranty. Read and follow the safety instructions that came with the product.

- 1 Remove the required sled from the system. See "Sled Configuration" on page 101.
- 2 Loosen the four captive screws on the heat sink .

- 3 Remove the heat sink/shroud assembly by tilting the backend up to clear the shroud from under the sled flange and then lift upwards ②.

Figure 3-27. Removing a Heat Sink/Shroud



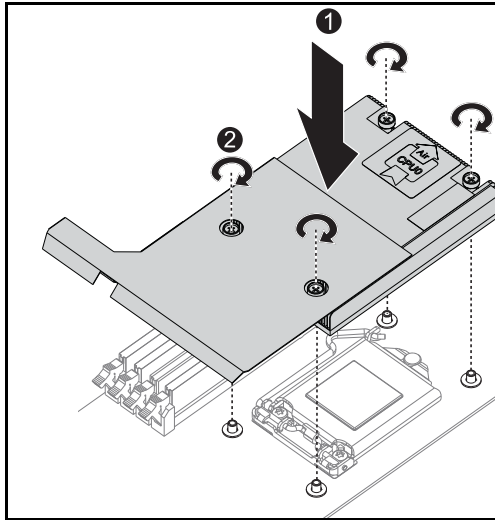
Installing a Heat Sink/Shroud

- 1 Use a lint-free cloth, remove thermal grease from the heat sink.
- 2 Apply new thermal grease evenly to the center of the top new processor.

△ CAUTION: Using excess thermal grease can cause grease to contact the processor shield, which can cause contamination of the processor socket.

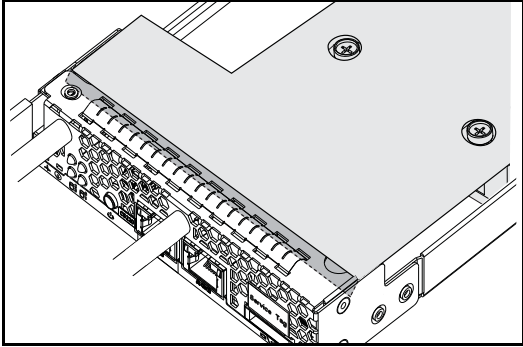
- 3 Position heat sink/shroud assembly at a slight tilt to ensure the heat sink/shroud is inserted below the sled flange (see final installed view), then lower the assembly onto the four supporting posts on the motherboard **1**.
- 4 Align the four screws of the heatsink to the four threaded posts and tighten the four screws **2**.

Figure 3-28. Installing a Heat Sink/Shroud



Final installed view shown in the following illustration.

Figure 3-29. Final Installed View of a Heat Sink/Shroud



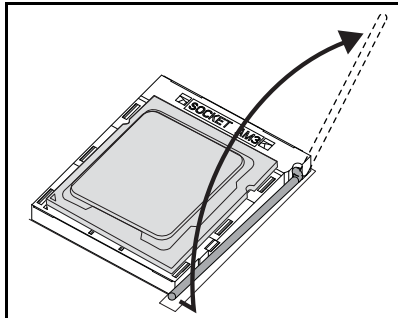
Processors

Removing a Processor

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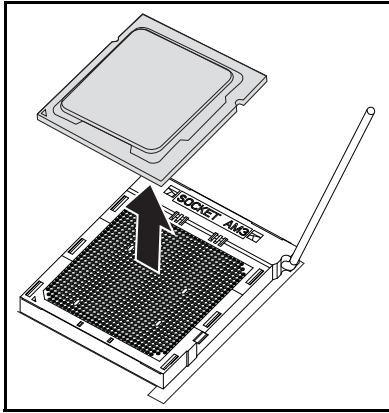
- 1 Remove the heatsink. See "Removing a Heat Sink/Shroud" on page 119.
- 2 Release the retention bar.

Figure 3-30. Releasing the Retention Bar



- 3 Remove the processor.

Figure 3-31. Removing a Processor

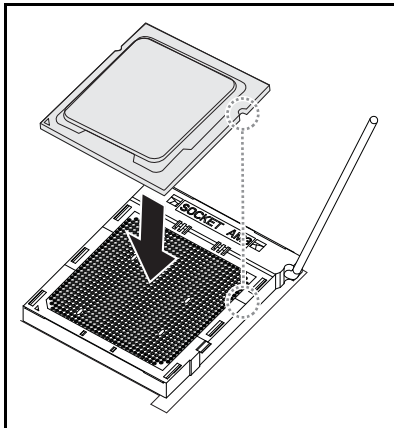


Installing a Processor

⚠ CAUTION: Positioning the processor incorrectly can permanently damage the system board or the processor. Be careful not to bend the pins in the socket.

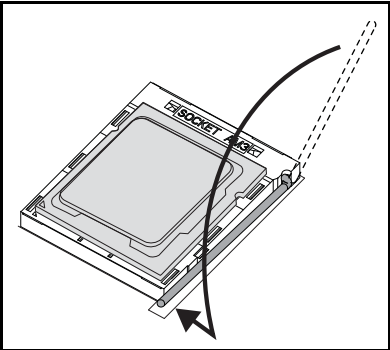
- 1 Place the new processor into the socket.

Figure 3-32. Installing a Processor



- 2 Close the retention bar.

Figure 3-33. Securing the Retention Bar



Troubleshooting

Troubleshooting Sequence

Server Boot Issues

System Does Not Boot After Initial Installation

Power Connector Not Plugged In

Memory Issues

Monitor Issues

Power Supply and Chassis Issues

Cable Issues

Electrical Short or Overload

Defective Components

System Does Not Boot After Configuration Changes

Hardware Changes

Software Changes

BIOS Changes

Viewing System Event Logs for Investigation

Installation Problems

Troubleshooting External Connections

System Does Not Boot After Initial Installation

Power Connector Not Plugged In

If the power supply cable is not plugged into the system board processor power connector, the system cannot boot up, even though chassis front panel LEDs and the fan may be operational. Verify that the power connections are good.

Memory Issues

If you have installed incompatible memory modules, the system may not boot. Verify the memory you've installed has been tested with your system board. If the installed memory is compatible, remove and reinstall the memory modules.

Defective memory modules may cause boot errors. To isolate a specific memory module as defective, boot the system with just one memory module installed at a time.

Monitor Issues

Monitor configurations can cause boot failure. Run through the following checklist to verify monitor operation:

- Ensure the monitor is plugged in and turned on.
- Ensure all cables are connected properly between the monitor and the system.
- Check that the brightness and contrast controls on the monitor are not too low.

Most monitors employ indicator LEDs showing status. Refer to the monitor's documentation to confirm operation. If the problem still persists, test or replace the monitor on a different AC outlet or system.

Power Supply and Chassis Issues

- Verify if the chassis and power supply are compatible with the processor model.

Table 4-1. Supported Processor List on the PowerEdge C5230

	Intel Processors	12-Sled SKU
Intel Xeon E3-1200v3	Intel Xeon E3-1280v2	Y
Product Family	Intel Xeon E3-1240v3	Y

Cable Issues

Ensure that all cable connections, both internal and external, are attached correctly and securely.

Electrical Short or Overload

Remove non-essential items such as extra controller cards or IDE/ATAPI devices to check for shorts and over-loads. If the system boots correctly, there may be a short or overload associated with one of the components. Replace each of the non-essential items one at a time to isolate which one is causing the problem.

If the problem occurs even after removing the non-essential components, the problem has to be with the system board, power supply, memory, or processor.

Defective Components

Defective components, especially processor and memory, can cause system boot issues.

- Swap the memory modules with known good memory. Verify correct operation of the suspected memory in a known working system.
- Swap the processor with a known good processor. Verify correct operation of the suspected processor in a known working system.

System Does Not Boot After Configuration Changes

Hardware Changes

If the system does not boot after making changes to hardware or adding new components, verify that the component installed is compatible with the system.

Software Changes

If you recently installed new software or new device drivers, try booting into Safe Mode and uninstall the new software or driver.

If you can now boot normally, there may be a compatibility issue between the new software or driver and some component in your system. Contact the software manufacturer for assistance.

BIOS Changes

Changes to some advanced BIOS settings (such as those found in the "Advanced Menu" on page 18) can cause boot issues. Changes to Advanced BIOS settings should only be made by experienced users.

If the BIOS Setup Utility is accessible by pressing F2 during boot, reset the BIOS to factory defaults by pressing F9. Save and exit the BIOS Setup (see "Start Menu" on page 11 for more details).

If you cannot access the BIOS Setup Utility, clear the CMOS by performing the following steps:

- 1 Turn off the system. Do not unplug the power cord.
- 2 Open the system.
- 3 Take the jumper and install on J18, covering pin1 and 2, then remove to reset/clear CMOS.
- 4 Remove AC power.
- 5 Wait 5 seconds.
- 6 Move the jumper back to default position, covering pins 1 and 2.
- 7 Replace the chassis cover and turn on the system.

The CMOS is now cleared and can be reset by going into BIOS setup.

Viewing System Event Logs for Investigation

If the front panel LED blinks for 30 to 60 seconds upon applying AC power to the power supply, the baseboard management controller (BMC) is initializing. If not, then the BMC is not functioning. If the BMC is working, try to gather system event log (SEL) information for investigation. For more information, see "View System Event Log" on page 56.

Installation Problems

Perform the following checks if you are troubleshooting an installation problem:

- Check all cable and power connections (including all rack cable connections).
- Unplug the power cord, and wait one minute. Then reconnect the power cord and try again.
- If the network is reporting an error, see if there is enough memory installed and disk space available.

- Remove all peripherals, one at a time, and try to turn on the system. If after removing an option the system works, you may find that it is a problem with the option or a configuration problem between the peripheral and the system. Contact the option vendor for assistance.
- If the system does not turn on, check the LED display. If the power LED is not on, you may not be receiving AC power. Check the AC power cord to make sure that it is securely connected.

Troubleshooting External Connections

Loose or improperly connected cables are the most likely source of problems for the system, monitor, and other peripherals (such as a printer, keyboard, mouse, or other external device). Ensure that all external cables are securely attached to the external connectors on your system. See the system's hardware owner's manual for the back panel connectors on your system.

Update Utilities

This chapter provides information about the update utilities.

BMC Firmware Update

The BMC (Baseboard Management Controller) firmware can be updated using various ways, including of remotely or locally, and can be achieved by IPMI command or by utilities. The update should be taken only if necessary.

Firmware Recovery Utility-SOCFLASH Utility

For BMC recovery, the utility SOCFLASH is used. If irregularities occur. SOCFLASH can be also used as the regular BMC Update with or without erasing user configuration data.



NOTE: All files and firmware are provided with each release package.

The format for SOCFLASH version 1.00.02 or later is:

```
socflash [operand]
```

operand list

- if=the name of the update file
- of=the name of the backup file

- cs= to set the chip select
AST2050: 2; default: get from SCU trapping.
- flashtype=the flash chip type
2:SPI
- skip=type the skip size in bytes at the start of input file (default=0)
- offset = type the offset in bytes at the start of the flash (default=0)
- count= type the size in bytes copy to the flash (default=the size of the flash)
- option=f|2|c
 - skip the comparison of flash data and force to update
 - use chip erase instead of sector erase
 - reset scratch
 - two flash update support

AST2050: two SPI solution: 1st SPI is on CS2; 2nd SPI is on CS0

Examples:

Flash All without Saving user configuration Data:

```
C:\socflash \dosflash>socflash cs=2 option=fc
if=firm.bin
```

Instructions for Linux SOCFLASH linux.sh:

Change directory to ./socflash

Execute sh ./linux.sh on Local System with Linux OS.

```
[root@localhost ~ socflash]# ./linux.sh
```

After the procedure is complete, wait 90 seconds for BMC to reset.

Instructions for DOS SOCFLASH dos.bat:

Change directory to .\socflash

Execute dos.bat on Local System with DOS.

```
c:\socflash\> dos.bat
```

After the procedure is complete, wait 90 seconds for BMC to reset.

Instructions for Windows 2008 64bit win.bat:

Change directory to `.\socflash`

Execute `win.bat` on Local System with Windows OS.

After flashing is complete, wait 90 seconds for BMC to reset.

Updates Through TFTP/HTTP/FTP

Updating Through TFTP/HTTP/FTP

- 1** Get Reservation ID.

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x30  
0x01
```

```
> 01
```

- 2** Enable Remote Update.

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x30  
0x02 0x01 0x10 0x01 0x00 0x00 0x00 0xff
```

```
>10 01 00 01 01
```

- 3** Get Protocol.

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x30  
0x02 0x01 0x10 0x02 0x00 0x00 0x00 0xff
```

```
>10 02 00 01 07
```

- 4** Set URL.

HTTP Server Update

(Ex: `http://192.168.1.111/s2gv112.bin`)

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x30  
0x03 0x01 0x10 0x03 0x00 0x00 0x00 0x01 0xFF 0x68 0x74 0x74 0x70  
0x3A 0x2F 0x2F 0x31 0x39 0x32 0x2E 0x31 0x36 0x38 0x2E 0x31 0x2E  
0x31 0x31 0x31 0x2F 0x73 0x32 0x67 0x76 0x31 0x31 0x32 0x2E 0x62  
0x69 0x6E
```

ASCII code for URL - "`http://192.168.1.111/s2gv112.bin`"

Response: 21 written data length

FTP Server Update

(Ex: ftp://user:user@192.168.1.111/s2gv112.bin)

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x30
0x03 0x01 0x10 0x03 0x00 0x00 0x00 0x01 0xFF 0x66 0x74 0x70 0x3A
0x2F 0x2F 0x75 0x73 0x65 0x72 0x3A 0x75 0x73 0x65 0x72 0x40 0x31
0x39 0x32 0x2E 0x31 0x36 0x38 0x2E 0x31 0x2E 0x31 0x31 0x31 0x2F
0x73 0x32 0x67 0x76 0x31 0x31 0x32 0x2E 0x62 0x69 0x6E
```

ASCII code for URL - "ftp://user:user@192.168.1.111/s2gv112.bin"

Response: 2a written data length

TFTP Server Update

(Ex: tftp://192.168.1.111/s2gv112.bin)

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x30
0x03 0x01 0x10 0x03 0x00 0x00 0x00 0x01 0xFF 0x74 0x66 0x74 0x70
0x3A 0x2F 0x2F 0x31 0x39 0x32 0x2E 0x31 0x36 0x38 0x2E 0x31 0x2E
0x31 0x31 0x31 0x2F 0x73 0x32 0x67 0x76 0x31 0x31 0x32 0x2E 0x62
0x69 0x6E
```

ASCII code for URL - "tftp://192.168.1.111/s2gv112.bin"

Response: 21 written data length

Updating BMC Firmware Through Firmware Command

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x08
0x01 0x01 0x80 0x00
```

Response: 34 firmware update task ID

(force update, config)

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x08
0x01 0x01 0x80 0x01
```

Response: 34 firmware update task ID

(normal update, no config)

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x08
0x01 0x01 0x00 0x00
```

Response: 34 firmware update task ID

(normal update, config)

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x08  
0x01 0x01 0x00 0x01
```

Response: 34 firmware update task ID

Get Firmware Status.

```
ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x08 0x02  
<Task ID (ex: 0x34)>
```

Response: Status Code as followed:

0x00: Transmitting Image

0x01: Validating Image

0x02: Programming

0x03: Ready to Accept Image

0x04: USB Unit Stage

0x05: Connecting to server

0x80: General Error

0x81: Cannot establish connection

0x82: Path not found

0x83: Transmission Abort

0x84: Checksum Error

0x85: Incorrect Platform

0x86: Allocate memory failed

0x87: Virtual media detach failed

0xFF: Completed

Restart firmware while status code is 0xFF

```
>ipmitool -H <BMC IP Address> -I lanplus -U root -P root raw 0x06  
0x02
```

BIOS System Update

This section describes the use of the AMI BIOS Flash Utility for updating the system BIOS.

Firmware Update Utility-AMI Flash Utility

AMI Flash Utility can update the BIOS through local interface.

- 1 Boot into DOS/Microsoft Windows.
- 2 Execute 5230BIOS(version).exe.



NOTE: DOS does not support long file names. To use a file under DOS mode, rename it to fit the required file structure before executing the file.

BIOS Recovery Mode

The BIOS has an embedded recovery technique in the 'boot block'. In the event that the BIOS becomes corrupt the boot block can be used to restore the BIOS to a working state. The routine is called when the 'system block' of the BIOS is empty or corrupt. The restore routine when called accesses the USB drive looking for a file named 5230_REC.ROM.

This is the reason the USB drive light comes on and the drive appears to be in use. If the file (5230_REC.ROM) is found it is loaded into the 'system block' of the BIOS to replace the corrupted information.

To restore your BIOS, copy the most recent version of your system board's BIOS file to a USB key and rename it to 5230_REC.ROM.

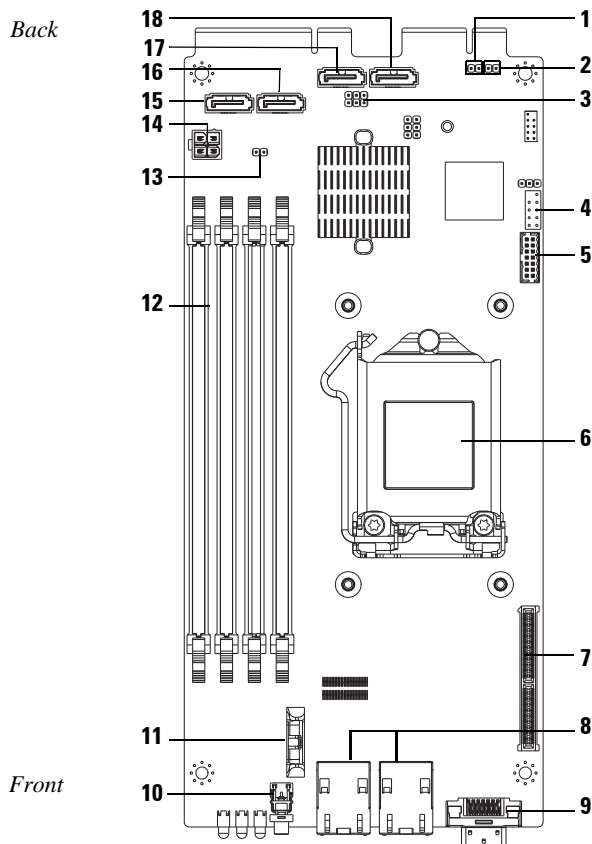
BIOS Recovery Flow

- 1 Rename the ROM file to 5230_REC.ROM and copy to the USB device.
- 2 Short the recovery jumper (JP13.3).
- 3 Power on the system.
The flash updating process starts automatically.
- 4 Remove the recovery jumper (J13.3).

Jumpers and Connectors

System Board Jumpers and Connectors

Figure 5-1. System Board Diagram



- | | | | |
|----|---|----|------------------------------|
| 1 | Disable BMC header (J27) | 2 | Password clear (J15) |
| 3 | ME recovery mode / BIOS recovery mode / flash descriptor security override header (J13) | 4 | Internal COM port |
| 5 | LPC connector | 6 | CPU socket |
| 7 | Mezzanine slot | 8 | NIC1/NIC2 RJ45 connector |
| 9 | Y cable connector (VGA + [USB x 2]) | 10 | Power button |
| 11 | Battery socket | 12 | DIMM slots |
| 13 | CMOS clear header (J18) | 14 | Power connector (debug only) |
| 15 | SATA connector HDD0 | 16 | SATA connector HDD1 |
| 17 | SATA connector HDD2 | 18 | SATA connector HDD3 |

Table 5-1. System Board Jumper Settings

Jumper	Default Setting	Function
JP13_12	Open	ME recovery mode Open: default Short: enable ME recovery
J13_34	Open	BIOS recover mode Open: default Short: enable BIOS recovery
J13_56	Open	Flash descriptor security override Open: security measures defined are set Short: security measures defined by BIOS are over-written
J15	Open	BIOS password clear Open: default Short: clear BIOS clear
J18	Open	CMOS clear Open: default Short: clear CMOS

Table 5-1. System Board Jumper Settings (continued)

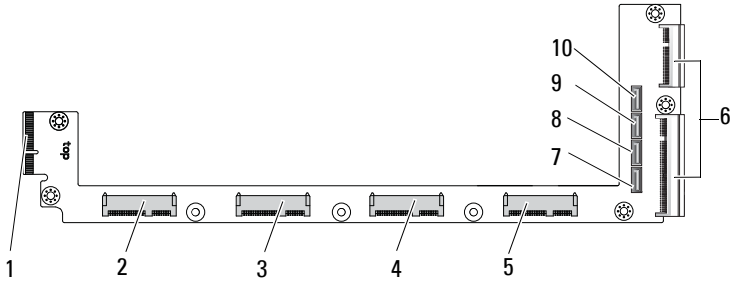
Jumper	Default Setting	Function
J27	Open	Disable ARM CPU operation Open: default Short: BMC disable



NOTE: BIOS version 1.0.2, Password, Legacy USB support and Quiet Boot Settings will not load default settings after clearing CMOS by jumper. BIOS version 1.0.3 or later, all default settings are loaded after a CMOS clear procedure. All user defined settings are lost.

2.5-inch Hard Drive Board Connectors

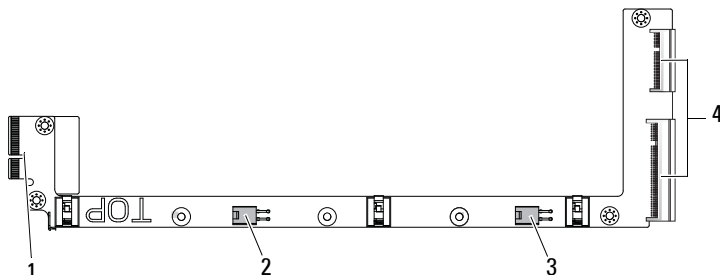
Figure 5-2. 2.5-inch Hard Drive Board



- | | | | |
|---|-----------------------------|----|-----------------------------|
| 1 | backplane connector | 2 | hard drive 0 connector |
| 3 | hard drive 1 connector | 4 | hard drive 2 connector |
| 5 | hard drive 3 connector | 6 | two board-edge connectors |
| 7 | hard drive 0 SATA connector | 8 | hard drive 1 SATA connector |
| 9 | hard drive 2 SATA connector | 10 | hard drive 3 SATA connector |

3.5-inch Hard Drive Board Connectors

Figure 5-3. 3.5-inch Hard Drive Board

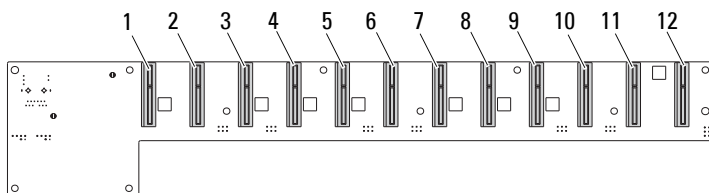


- | | | | |
|---|------------------------------|---|------------------------------|
| 1 | backplane connector | 2 | hard drive 0 power connector |
| 3 | hard drive 1 power connector | 4 | two board-edge connectors |

Backplane Connectors

12-Sled Backplane Front Connectors

Figure 5-4. 12-Sled Backplane Front Connectors

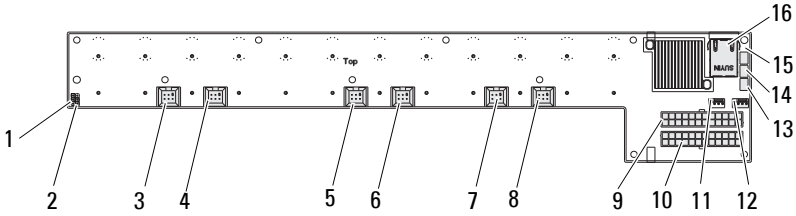


- | | | | |
|----|-------------------|----|-------------------|
| 1 | sled 1 connector | 2 | sled 2 connector |
| 3 | sled 3 connector | 4 | sled 4 connector |
| 5 | sled 5 connector | 6 | sled 6 connector |
| 7 | sled 7 connector | 8 | sled 8 connector |
| 9 | sled 9 connector | 10 | sled 10 connector |
| 11 | sled 11 connector | 12 | sled 12 connector |

12-Sled Backplane Back Connectors

Figure 5-5 shows the connectors on the back of the backplane.

Figure 5-5. 12-Sled SKU Backplane Back Connectors



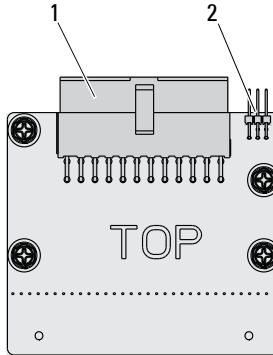
- | | | | |
|----|--------------------|----|-------------------|
| 1 | MD2 Jumper | 2 | MD1 Jumper |
| 3 | fan connector 1 | 4 | fan connector 4 |
| 5 | fan connector 2 | 6 | fan connector 5 |
| 7 | fan connector 3 | 8 | fan connector 6 |
| 9 | PSU 1 connector | 10 | PSU 2 connector |
| 11 | fan connector 7 | 12 | fan connector 8 |
| 13 | PMBus 2 connector | 14 | PMBus 1 connector |
| 15 | sideband connector | 16 | LAN connector |

Table 5-2. 12-Sled Backplane Jumper Positions

MD2	MD1	Mode
0	1	Normal
1	1	JTAG
1	0	Boot

Power Distribution Board Connectors

Figure 5-6. PDB Connectors



1 PSU connector

2 PMBus connector

PDB Power and SMBus Connectors

This section provides information on the PDB power and SMBus connector pin out.

Table 5-3. PDB Power and SMBus Connector Pin Out

Pin	Signal	Pin	Signal
1	+12V	2	+12V
3	+12V	4	+12V
5	+12V	6	+12V
7	+12V	8	+12V
9	+12V	10	CSHARE
11	PS_PRESENT_0	12	+12V
13	GND	14	GND
15	GND	16	GND
17	GND	18	GND
19	GND	20	GND

Table 5-3. PDB Power and SMBus Connector Pin Out

Pin	Signal	Pin	Signal
21	GND	22	P12V_STB
23	P12V_STB	24	GND
25	SMB_BP-_CLK	26	SMB_BP_DAT
27	SMB_PDB_ALRT_0/1_N	28	PS_ON_N
29	NA	30	PSGD0/1

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